LECTURE NOTES

ON

POWER ELECTRONICS

4th SEMESTER

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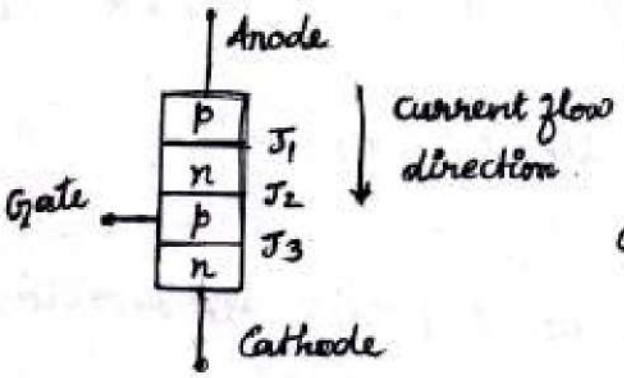
Structure, Operation and Characteristics of SCR

Thyristor is a 4-layered, 3-junction pnpn semiconductor switching device.

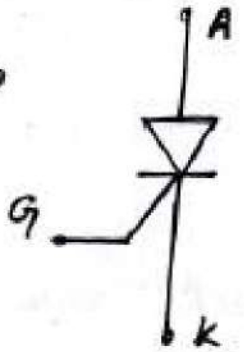
Has 3 terminals - Anode, Cathode and Gate.

SCR is an unidirectional device.

Schematic diagram



Circuit Symbol



The thyristor consists of four layers of alternate p-type & n-type silicon semiconductors forming three junctions J_1, J_2 & J_3.

The terminal connected to outer p-region forms anode 'A', the terminal connected to outer n region is called gate 'Cathode 'K'.

The Gate terminal is usually kept near cathode terminal.

SCR's are solid state devices, they are compact, possess high reliability and have low loss.

Power handling capability is more.

Operation.

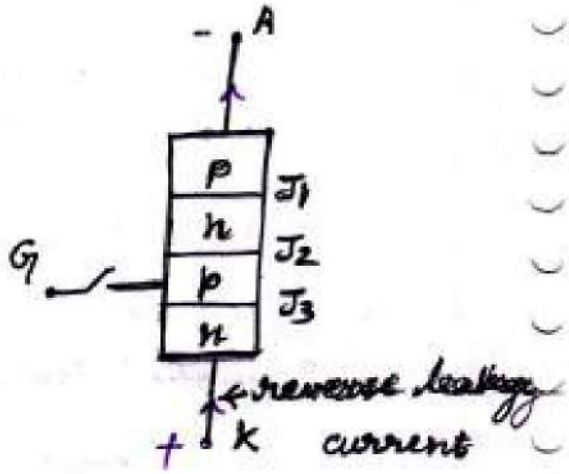
The thyristor has 3 basic modes of operation.

Reverse blocking mode

Forward blocking mode

Forward conduction mode.

Reverse blocking mode.



The switch S open (i.e., gate open)

Cathode is made positive with respect to anode.

∴ The thyristor is reverse biased.

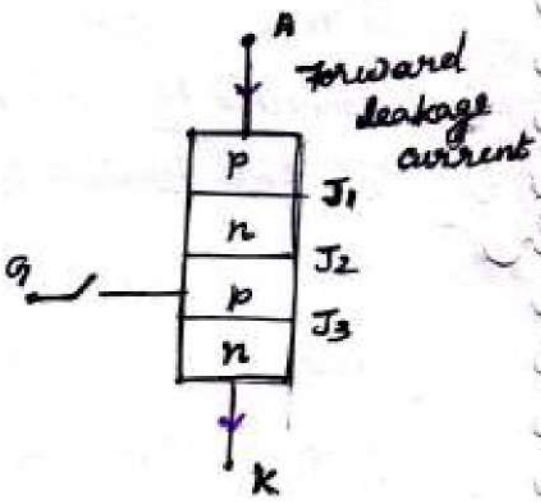
The junctions J_1, J_3 are reverse biased whereas junction J_2 is forward biased.

A small leakage current flows (of the order few mA or μA).

If the reverse voltage is ↑ed, then at reverse breakdown voltage V_{BR}, an avalanche occurs at J_1 & J_3 & the reverse current increases rapidly.

The large reverse current will lead to thyristor damage.

Forward blocking mode.



Here anode is positive with respect to cathode, with gate circuit open.

The thyristor is said to be forward biased.

Junctions J_1, J_3 are forward biased whereas junction J_2 is reverse biased.

In this mode, a small current, called forward leakage current flows.

As the forward leakage current is small, SCR offers a high impedance.

Therefore, a thyristor can be treated as an open switch even in the forward blocking mode.

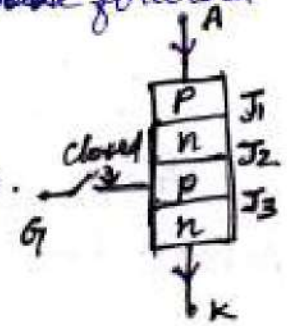
Forward Conduction mode.

A thyristor can be brought from forward blocking mode to forward conduction mode by applying

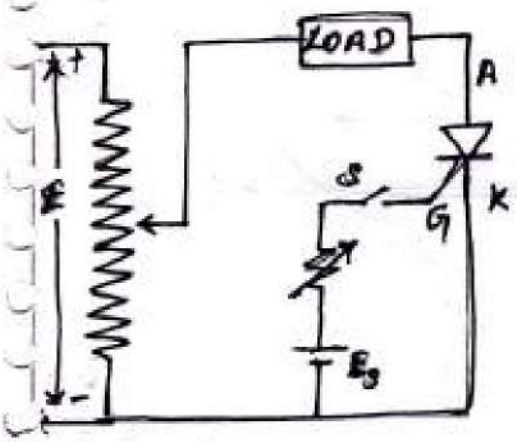
i) a positive gate pulse between gate & cathode. (OR)

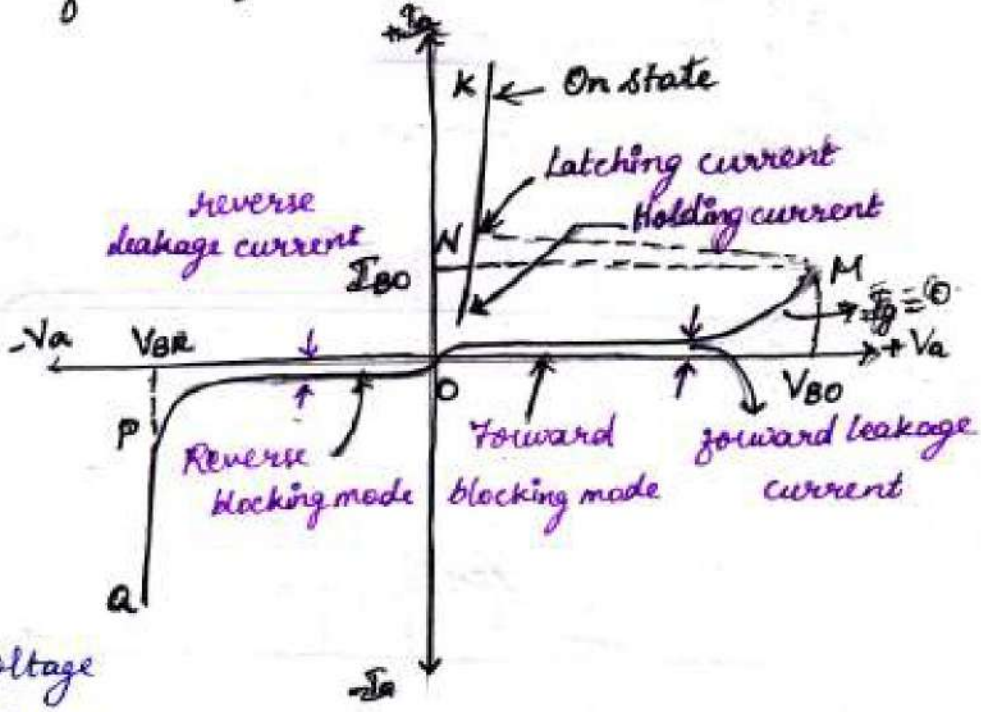
ii) by increasing the anode to cathode voltage above forward breakover voltage (V_{BO}).

After this breakdown, thyristor gets turned on.



4c I-V characteristics of a thyristor.





V_{BO} - Forward breakover voltage

V_{BR} - Reverse breakdown voltage.

I_g - Gate current.

V_a - Voltage across anode & cathode.

Latching current (I_L)

Minimum anode current required to bring the device into conduction.

Holding current (I_H)

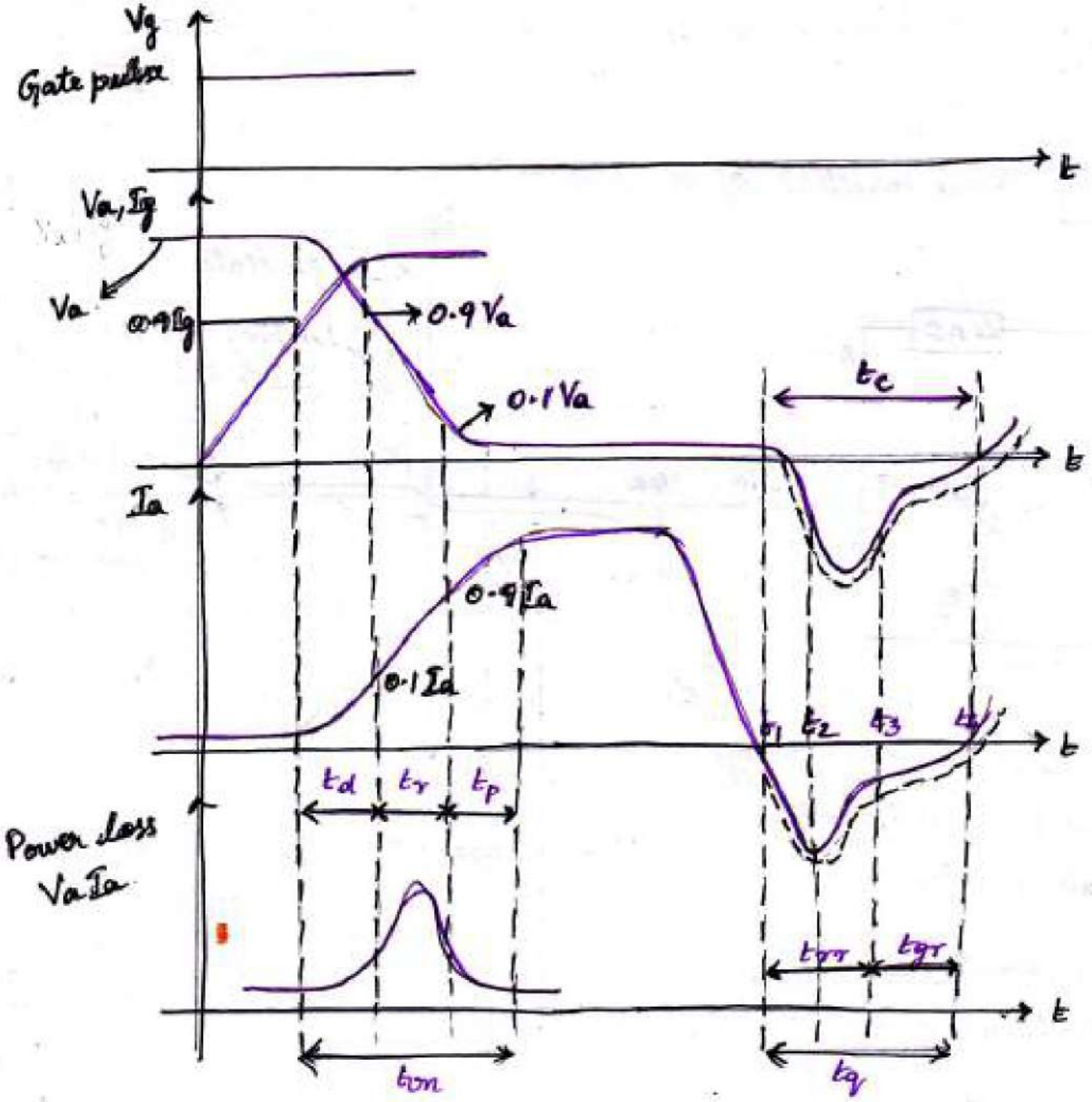
Minimum anode current required to maintain the device in 'ON' state.

I_L should always be higher than I_H ie, $I_L > I_H$.

Thyristor - turn ON methods

i) Forward voltage method
ii) Thermal triggering
iii) Radiation / Light triggering
iv) $\frac{dv}{dt}$ triggering
v) Gate pulse triggering
vi) Forward voltage triggering

Switching Characteristics of SCR



$t_{on} = t_d + t_r + t_p$

$t_q = t_{rr} + t_{gr}$

t_{on} - On time
t_q - off time
t_d - delay time
t_r - rise time
t_p - spread time
t_{rr} - reverse recovery time
t_{gr} - gate recovery time.

SCR is capable of being switched from fwd blocking state to fwd conduction state.

The transition from 1 state to the other does not take place instantaneously & it occupies the finite period of time. This period is known as transient period / transition time.

The variation of voltage & current during turn ON & OFF process gives the dynamic (or) switching characteristics.

SCR can be turn ON by applying +ve gatepulse blw G & K.

Now the SCR switches from fwd blocking to fwd conduction state.

However, it takes some time for transition.

Turn-on time is divided into process
i) delay time (t_d)
ii) rise time (t_r)
iii) spread time (t_p)

Delay time (T_d)

It is measured from the instant at which gate current reaches I_g (90% of I_g) to the instant at which anode current reaches $0.1 I_a$.

It may also be defined as the time during which anode voltage falls from V_a to $0.9 V_a$.

I_a → final value of anode current
I_g → " " " gate "
V_a → initial " " anode voltage.

The delay time can be red by applying high gate current & more forward voltage blw anode & cathode.

Rise time (t_r)

It is the time taken by the anode current to rise from 0.1 I_a to 0.9 I_a. (ie, 10% to 90% of I_a)

Also it can be defined as the time required for the forward blocking voltage to fall from 0.9 V_a to 0.1 V_a.

Spread time (t_p)

It is the time taken by the anode current to rise from 0.9 I_a to I_a.

Also defined as time for the fwd blocking voltage to fall from 0.1 V_a to its fwd on state vol drop (1 to 1.5 volt)

Turn-off process

Thyristor turn off means that it has changed from on to off state & is capable of blocking fwd voltage.

This dynamic process of SCR from fwd conducting state to fwd blocking state is called commutation / turn-off process.

Once, the thyristor is ON, the gate losses its control.

The SCR can be turned off by reducing the anode current below holding current.

turn off time (t_q)

During time t_q, all the excess carriers from the 4 layers of SCR must be removed.

This removal of excess carriers consists of sweeping out of holes from outer P layer & electrons from N layer. The carriers around the junction (J_2) can be removed only by recombination.

Reverse recovery time (t_{rr})

At instant t_1, anode current becomes zero & after t_1, I_a builds up in the reverse direction.

The reason for reversal of anode current is due to the presence of carriers stored in the four layers during conduction.

In order to turn-off the thyristors, these carriers should be removed.

Reverse recovery current removes carriers from junctions J_1 & J_3 between the instants T_1 & T_3.

At T_2, when about 60% of the stored charges are removed from the outer layers, & the t_{rr} ↓s & starts decaying.

Gate recovery time (t_{gr})

At T_3, the excess carriers in J_1 & J_3 are removed & they can block reverse voltage.

At the end of T_3, the middle junction J_2 still has some trapped charges.

The thyristor is unable to block the fwd vol.

These charges cannot flow through external circuit & can be removed only by recombination.

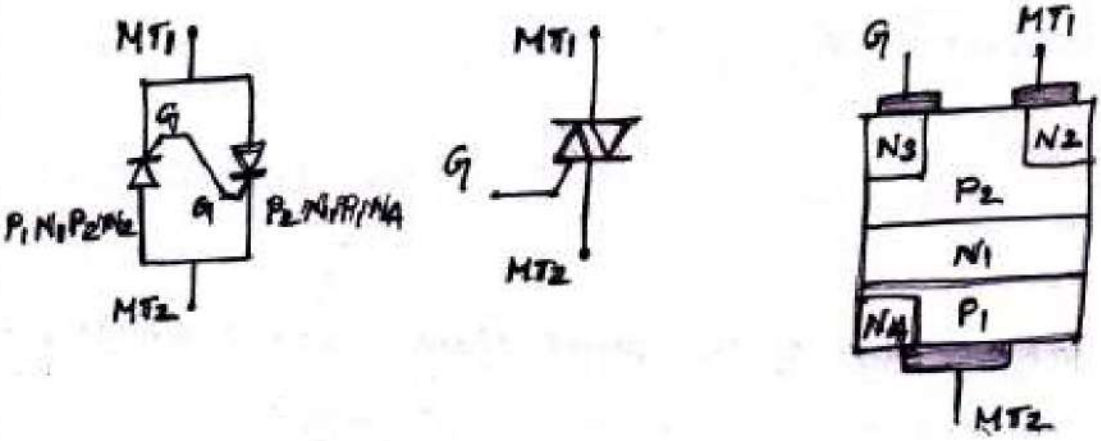
$\therefore$ $\boxed{T_q = t_{rr} + t_{gr}}$

Structure, Operation & Characteristics of TRIAC

TRIode & AC.

Bidirection thyristor with three terminals (MT1, MT2 & G)

Two thyristors connected antiparallely (ie., back to back)



The triac can conduct in both the directions, the terms anode & cathode are not applicable to triac.

Its three terminals are represented as MT1 (Main terminal 1), MT2 (Main terminal 2) and the gate by G.

The Gate G is near terminal MT1 if it is connected to N3 & P2 as well as to.

Similarly, terminal MT1 is connected to P2 & N2 ; &

terminal MT2 is connected to P1 & N4.

Triac can be turned on in each half cycle of the applied voltage by applying a positive or negative voltage to the gate with respect to MT1.

It operates in 4 modes.

Forward blocking mode

Forward Conduction mode

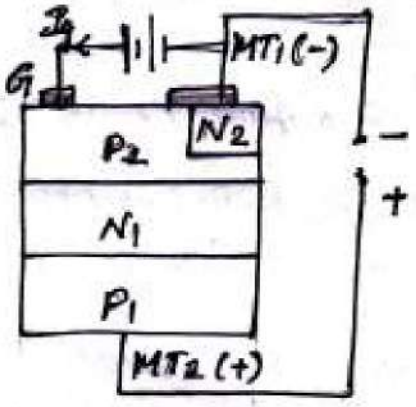
Reverse blocking mode

Reverse Conduction mode.

Based on the biasing given to the terminals,

Mode 1:

MT_1 : -ve MT_2 : +ve G : +ve



P_1N_1, P_2N_2 → FB

N_1P_2 → RB.

When G - +ve w.r to MT1,

I_g flows through P_2N_2 junction mainly.

When I_g has injected sufficient charge in P_2 layer, RB junction P_2 breaks down ~~fault & therefore~~ triac operates in I quadrant.

Triac now starts conducting through $P_1N_1P_2N_2$ layers.

Under this condition, triac operates in I quadrant.

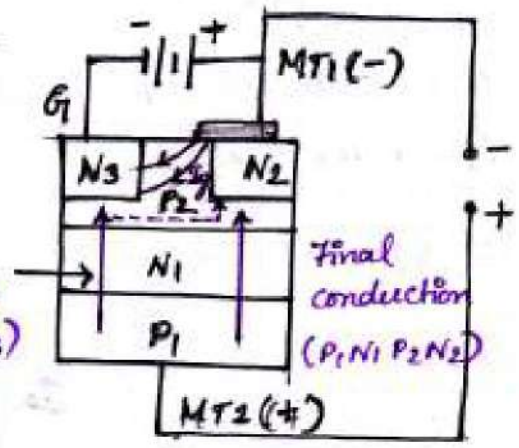
Mode 2:

MT_1 : +ve MT_2 : +ve G : -ve

When gate terminal is -ve w.r.to MT_1, I_g flows through P_2N_3 junction.

N_1P_2 - FB

∴ Initially, triac starts conducting through $P_1N_1P_2N_3$ layers.



The voltage drop across this path falls but potential of layer blw N_3 rises towards the anode potential of MT_2.

The potential gradient exists across P_2 [as right hand portion of P_2 is clamped]

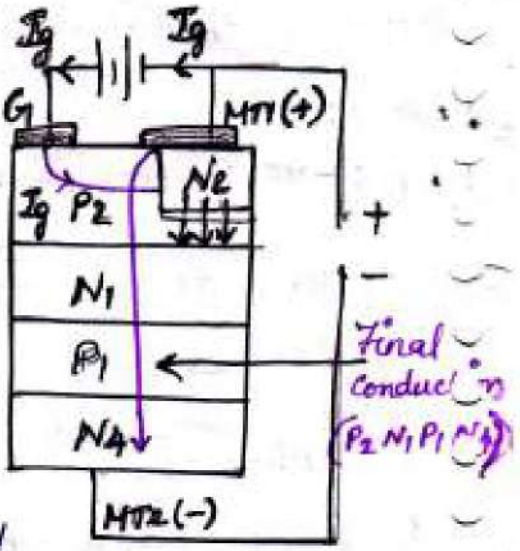
Left hand region of P_2 → higher potential

Right " " " " → Lower "

As a consequence, right hand part of triac consisting of $P_1N_1P_2N_2$ begins to conduct.

Mode 3 :

MT_1 : +ve MT2 : -ve G_1 : +ve



Ig flows from P_2 to N_2.

RB jn $N_1 P_1$ is broken.

Finally, $P_2 N_1 P_1 N_4$ is turned on completely.

$P_2 N_2$ – FB.

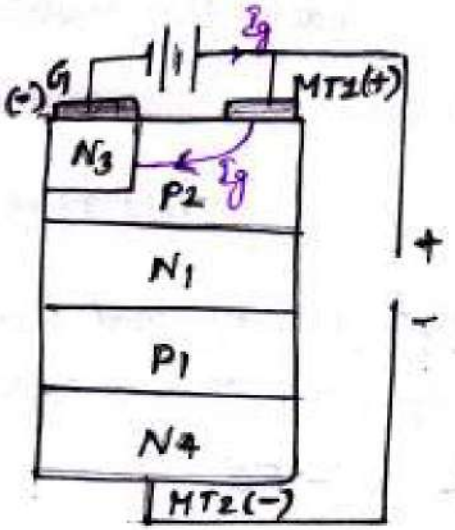
Layer N_2 injects e^-s into P_2 layer (dotted arrows).

As a result, RB jn $N_1 P_1$ breaks down.

Eventually, $P_2 N_1 P_1 N_4$ – on.

Mode 4 :

MT1 : +ve MT2 : -ve G : -ve

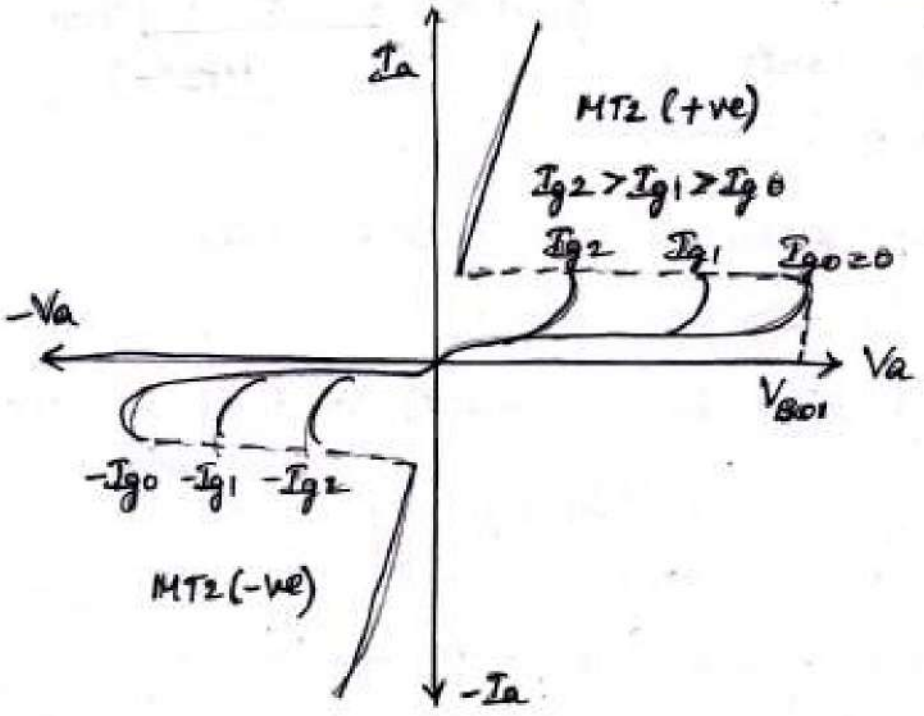


Ig flows from P_2 to N_3.

$N_1 P_1$ – broken & finally

$P_2 N_1 P_1 N_4$ – on.

Static VI Characteristics.



Power MOSFET's (Metal-oxide-semiconductor field-effect transistor)

Voltage controlled device.

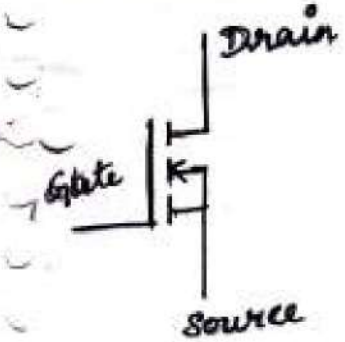
Unipolar device.

Consists of 3 terminals drain (D), source (S) and gate (G).

2 types
- n-channel enhancement MOSFET. (most commonly used)
- p-channel enhancement MOSFET

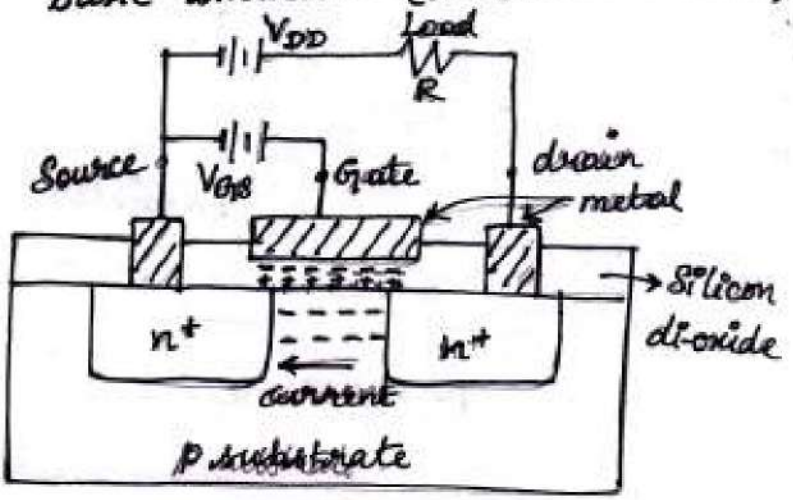
Symbol

n-channel



p-channel

basic structure (n-channel MOSFET)



On p-substrate, two heavily doped n^+ regions are diffused.

An insulating layer of silicon dioxide (SiO_2) is grown on the surface.

This insulating layer is etched in order to embed metallic source and drain terminals.

A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source & drain terminals.

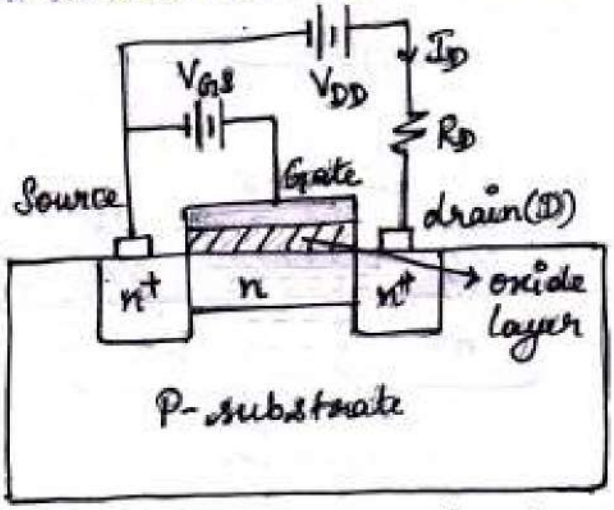
Power Mosfets requires base current for current flow in the collector & also it requires only a small I/p current.

The switching speed is very high & the switching times are of the order of nanoseconds.

Power Mosfets find applications in low power high frequency converters.

An n-channel enhancement-type Mosfet has no physical channel. When V_{GS} +ve, an induced voltage attracts the electrons from p-substrate & accumulate them at the surface beneath the oxide layer.

When V_{GS} is greater than or equal to a value known as threshold voltage V_T, a sufficient number of e^-s are accumulated to form a virtual n-channel and the current flows from the drain to source.



n-channel depletion type Mosfet

An n-channel depletion-type Mosfet is formed on a p-type silicon substrate.

The gate is isolated from the channel by a thin oxide layer.

The three terminals are called gate, drain & source.

The substrate is normally connected to the source.

The gate to source voltage V_{GS} could be either +ve or -ve.

If V_{GS} is negative, some of the e^-s in the n-channel are repelled & a depletion region is created below the oxide layer, resulting in a narrower effective channel & a high resistance from drain to source R_{DS}.

Therefore no current flows from drain to source, $I_{DS} = 0$.

The value of V_{GS} when this happens is called pinch-off voltage V_p.

Insulated Gate Bipolar Transistor (IGBT)

IGBT is a combination of both BJT and MOSFET.

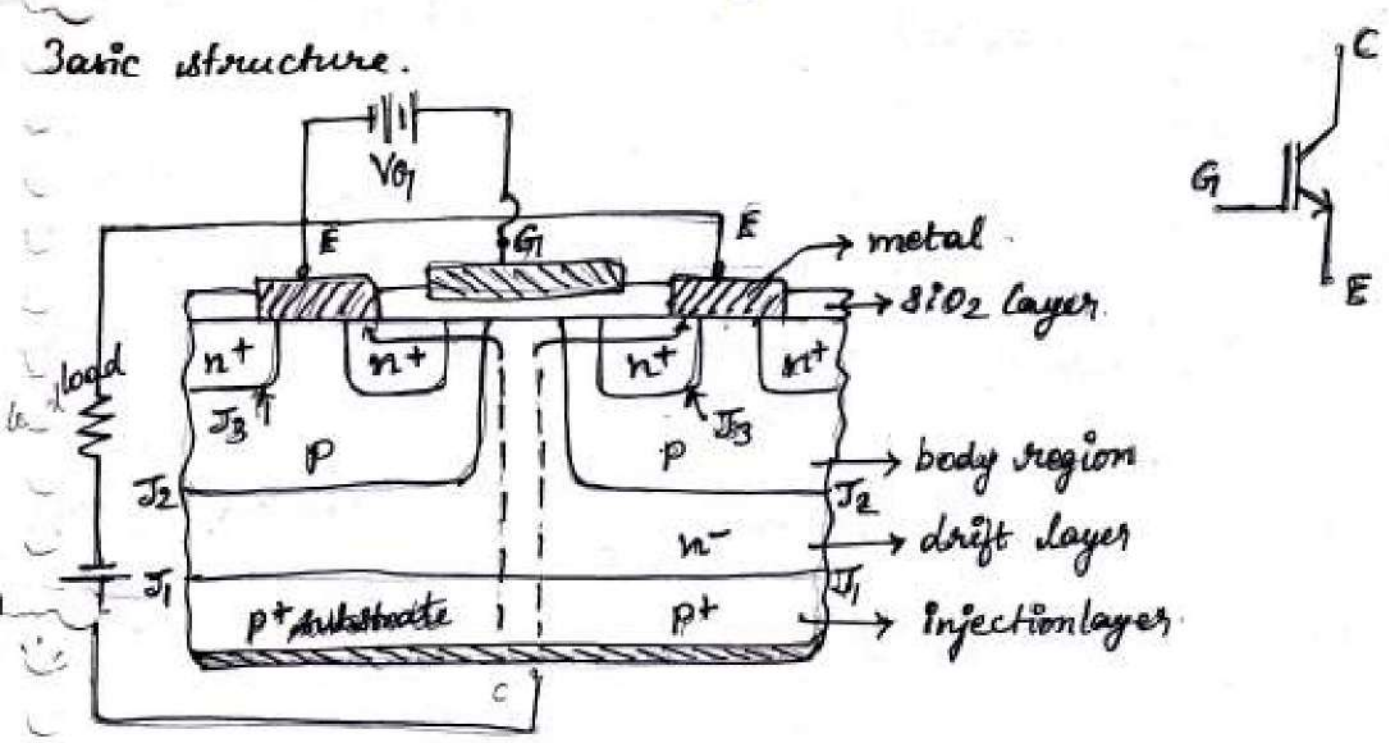
Thus IGBT possesses high input impedance like a power MOSFET and has low on-state power loss as in a BJT.

Further, IGBT is free from second breakdown problem present in BJT.

IGBT is also known as metal oxide insulated gate transistor (MOSIGT), conductively-modulated field effect transistor (COMFET) or gain-modulated FET (GEMFET).

Also called as insulated gate transistor (IGT).

Basic structure.



The construction of Mosfet is similar in structure as power Mosfet except a thing.

The major difference is that n^+ layer substrate at the drain in a Power Mosfet is substituted in the IGBT by a p^+ layer substrate called collector C.

In IGBT, p^+ substrate is called injection layer because it injects holes into n^- layer.

The n^- layer is called drift region.

The thickness of n^- layer determines the voltage blocking capability of IGBT.

The p layer is called body of IGBT.

The n^- layer in between p^+ & p regions serves to accomodate the depletion layer of pn^- junction (J_1, J_2)

Working

When collector is made positive with respect to emitter, IGBT gets forward biased.

With no voltage between gate & emitter, two junctions between n^- region & p region (J_1, J_2) are reverse biased; so no current flows from collector to emitter.

When gate is made positive w.r.t. to emitter by voltage V_{GE}, with gate-emitter voltage more than the threshold voltage $V_{GE(TH)}$ of IGBT, an n-channel or inversion layer, is formed in the upper part of p region just beneath the gate, as in power Mosfet.

This n-channel short ckts the n^- region with n^+ emitter regions.

Electrons from n^+ emitter begin to flow to n^- drift region through n-channel.

As IGBT is fwd biased with collector positive & emitter negative, p^+ collector region injects holes into n^- drift region.

With this, the injection carrier density in n^- drift region is considerably & as a result, conductivity of n^- region enhances significantly.

Therefore, IGBT gets turned on & begins to conduct forward current I_C.

What is latchup in IGBT?

IGBT switching characteristics.

Turn-on time

It is defined as the time blw the instants of forward blocking to forward on-state.

Turn-on time is composed of delay time (t_{dn}) and rise time (t_r).

ie, $\boxed{t_{on} = t_{dn} + t_r}$

Delay time (t_{dn})

It is defined as the time for the collector-emitter voltage to fall from V_{CE} to $0.9\,V_{CE}$. $V_{CE} \rightarrow$ Initial collector-emitter vol.

It is also defined as the time for the collector current to rise from its initial leakage current I_{CE} to $0.1\,I_C$.

$I_C \rightarrow$ final value of collector ct.

Rise time (t_r)

It is the time during which collector-emitter voltage ~~volto~~ falls from $0.9\,V_{CE}$ to $0.1\,V_{CE}$.

It is also defined as the time for the collector current to rise fr $0.1\,I_c$ to its final value I_c.

After time t_{on}, the I_c & V_{CE} falls to small value called conduction drop = V_{CES} (S here denotes → saturated value)

Turn-off time

It consists of 3 intervals delay time (t_{df}), initial fall time (t_{f1}) and final fall time, (t_{f2}).

ie, $\boxed{t_{off} = t_{df} + t_{f1} + t_{f2}}$

Delay time (t_{df})

It is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}.

As V_{GE} falls to V_{GET} during t_{df}, the collector current falls from I_C to $0.9\,I_C$.

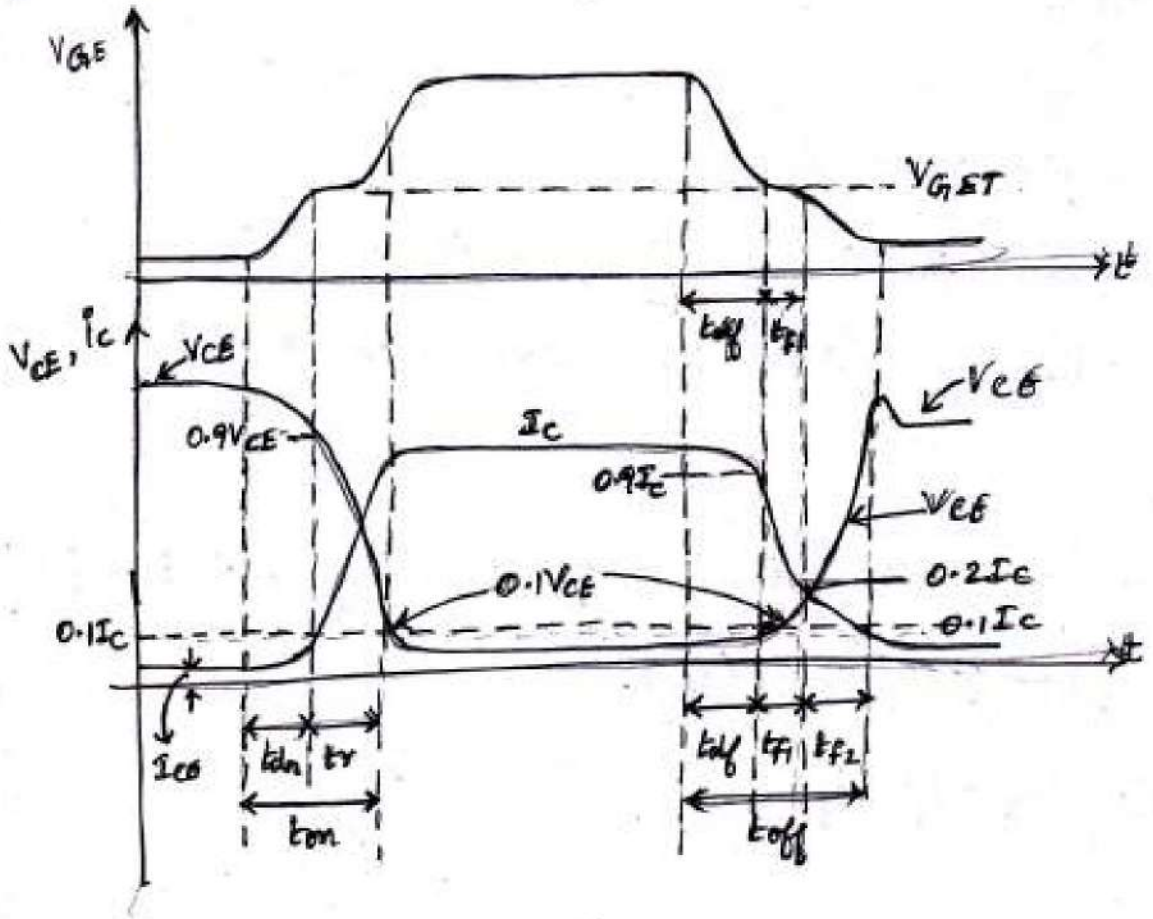
At the end of t_{df}, collector-emitter voltage begins to rise.

First fall time (t_{f1})

- defined as the time during which I_C falls from 90 to 20% of its value I_C.
- also defined as the time during which V_{CE} rises from V_{CES} to $0.1\,V_{CE}$.

Final fall time (t_{f2})

- defined as the time during which I_C falls from 20 to 10% of I_C
- also defined as the time during which V_{CE} rises from $0.1\,V_C$ to final value V_{CE}.



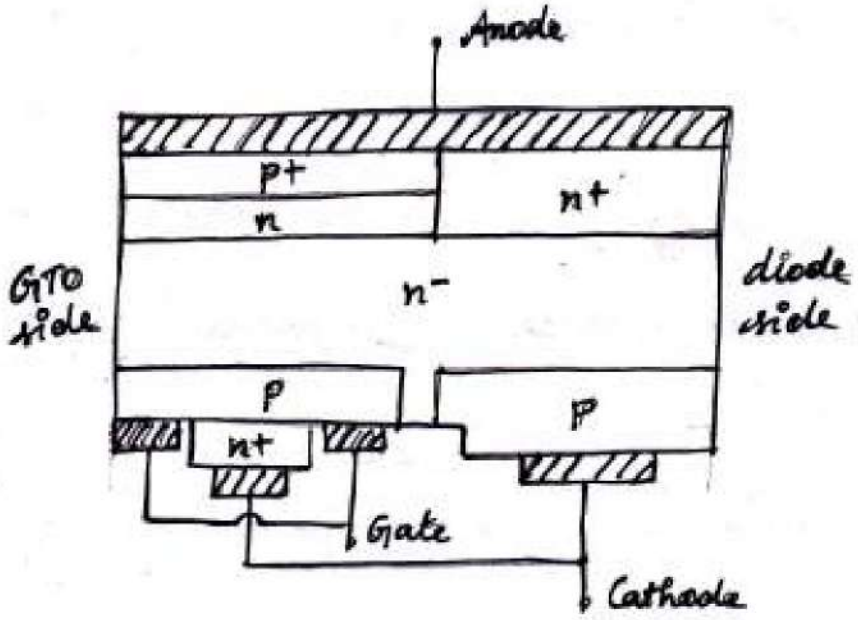
IGCT (Integrated Gate Commutated Thyristor)

The IGCT integrates a gate-commutated thyristor (GCT) with a multilayered printed circuit board gate drive.

The GTO is a hard-switched GTO with a very fast and large gate current pulse, as large as the full rated current, that draws out all the current from the cathode into the gate in about 1 µs to ensure a fast turn-off.

The internal structure & equivalent circuit of a GCT are similar to that of a GTO.

Cross section of IGCT with a reverse diode



An IGCT may also have an integrated reverse diode, as shown by the n^+n^-p junction on the right side of the IGCT structure.

Similar to a GTO, an MTO (MOS turn-off thyristors) & an ETO (Emitter turn-off thyristors), the n^- buffer layer evens out the voltage stress across the n^- layer, reduces the thickness of n^- layer, & the on-state conduction losses, & makes the device asymmetric.

The anode p-layer is made thin & lightly doped to allow faster removal of charges from the anode-side during turn-off

Turn-on

Similar to GTO, the IGCT is turned on by applying the turn-on current to its gate.

Turn-off

The IGCT is turned off by a multilayered gate driver ckt board that can supply a fast rising turn-off pulse.

Due to a very-short duration pulse, the gate-drive energy is greatly reduced and the gate-drive energy consumption is minimized.

The gate-drive power requirement is red by a factor of five compared with that of the GTO.

To apply a fast-rising & high-gate current, the IGCT incorporates a special effort to reduce the inductance of the gate circuitry as low as possible.

This feature is also necessary for gate-drive circuits of the MTO & ETO.

Gate turn off thyristor (GTO)

Refer Rashid.

Adv of GTOs over SCR & BJT

Conventional thyristors (CTs) can be easily turned on by +ve gate ctg.

The gate loses its control once it comes to on-state.

The CTs can now be turned off by expensive & bulky commutation circuitry.

These drawbacks had led to the development of GTOs.

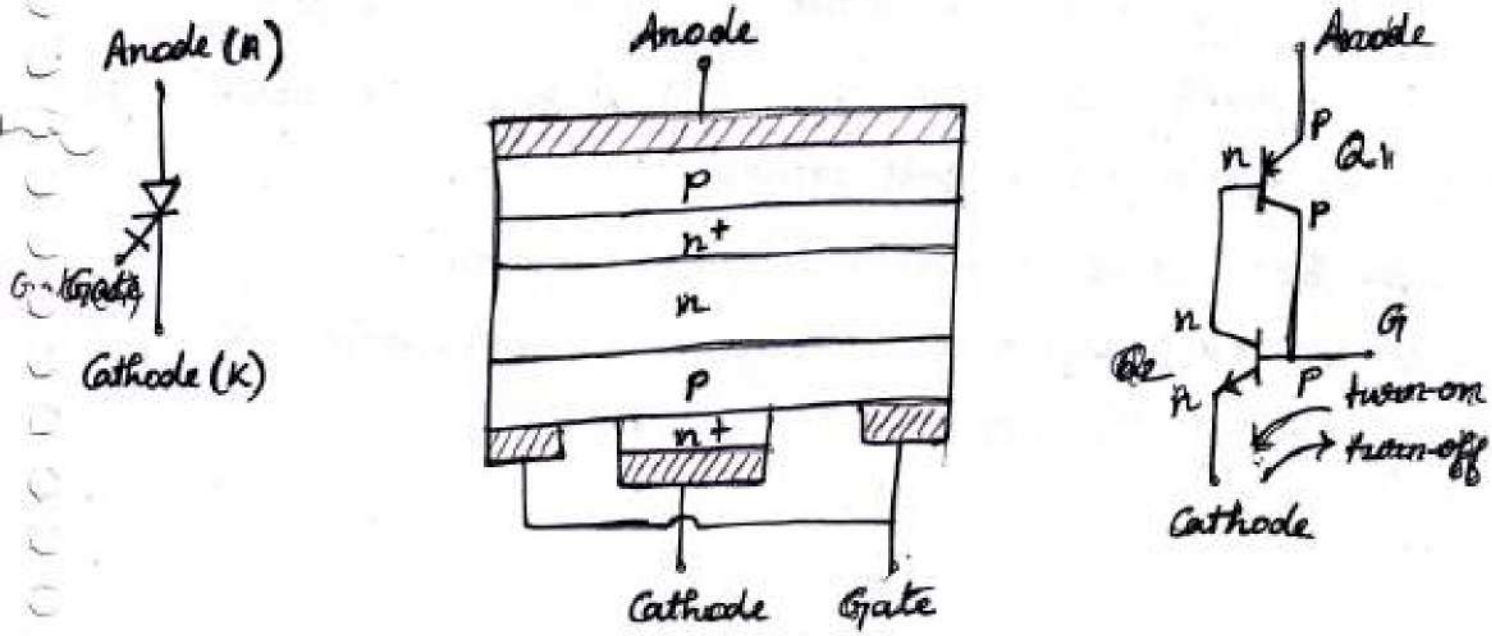
A GTO like an SCR can be turned on by applying +ve gate signal.

However, a GTO can be turned off by a -ve gate signal.

A GTO is a non-latching device & can be built with ctg & vol ratings similar to those of an SCR.

A GTO can be turned on by applying a short +ve pulse & turned off by a short -ve pulse to its gate.

It is a latch-on device, but it is also a latch off device.



(a) Symbol (b) Cross section (c) Equivalent circuit

A GTO is pnpn, three terminal device with anode (A), Cathode (k) & gate (G).

Compared to a CT, it has an additional n^+ layer near the anode that forms a turnoff ckt b/w the G & K in ||el with the turn-on gate.

Turn-on

The GTO has a highly interdigited gate structure with no regenerative gate.

As a consequence, a large initial gate trigger pulse is required to turn on.

Once the GTO is turned on, forward gate current must be continued for the whole of the conduction period to ensure the device remains in conduction.

Otherwise, the device cannot remain in conduction during the on-state period.

The on-state gate ct should be atleast 1% of the turn-on pulse to ensure that the gate doesnot latch.

Turn-off

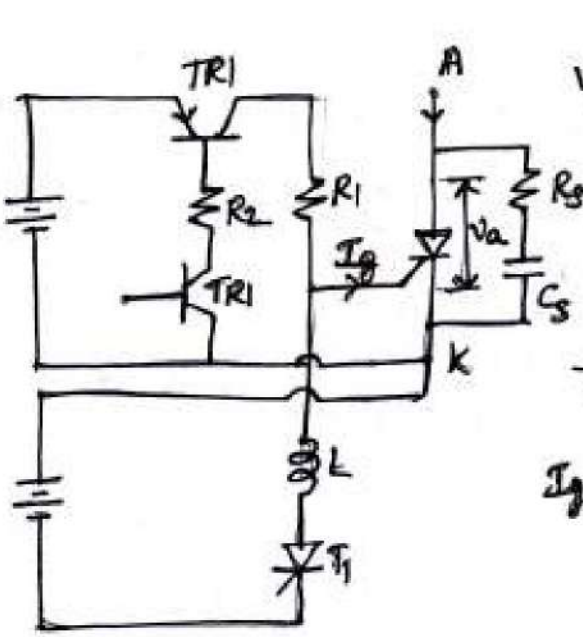
The turn-off process is quite diff from that in a CT.

For initiating the turn-off process in a GTO, a negative gate current is applied across gate-cathode terminals.

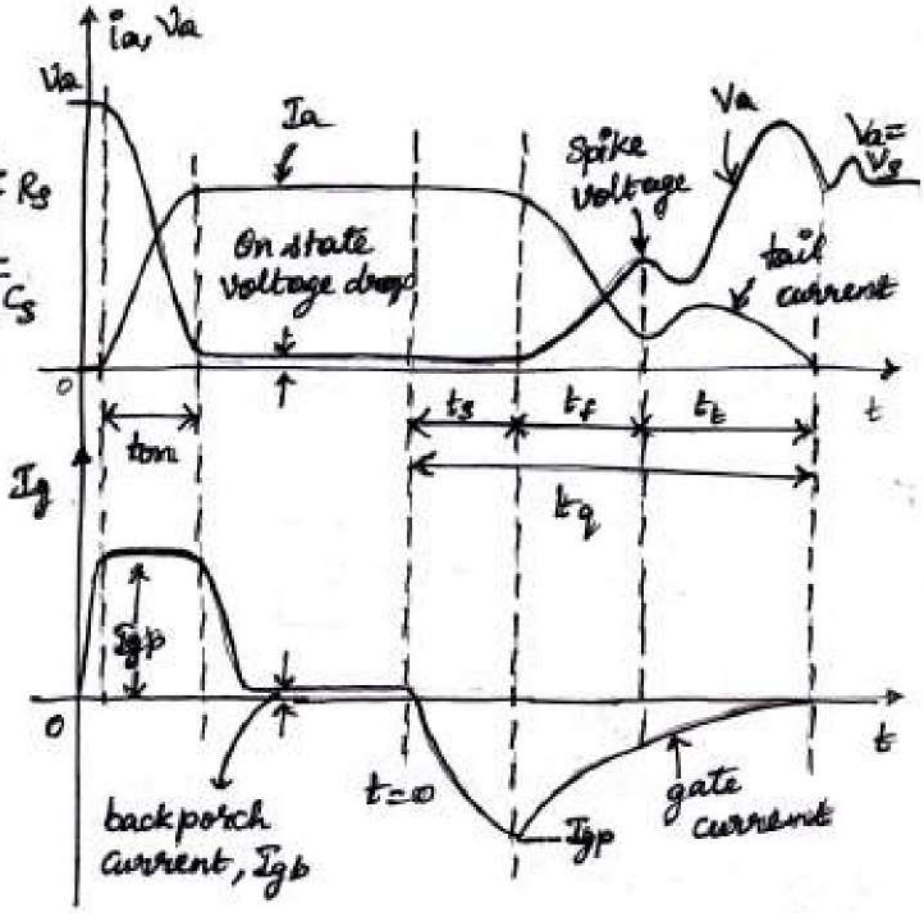
Q_2 must be brought out of saturation.

So, Q_2 would shift to active region & regenerative action would eventually turn-off the GTO.

Switching Characteristics of GTO.



a) Basic drive circuit



For turning-on a GTO, first transistor TR1 is turned on, this in turn switches on TR2 to apply a +ve gate-ct pulse to turn-on GTO.

For turning off the GTO, the turn-off ckt should be capable of outputting a high peak ct.

The turn-off process is initiated by gating thyristor T_1.

When T_1 is on, a large -ve gate current pulse turns off the GTO.

Gate turn-on

The gate turn-on time of GTO is made up of delay time, rise time, and spread time like a CT.

Further, turn-on time in a GTO can be red by ing its forward gate current as in a thyristor.

A steep-fronted gate pulse is applied to turn-on GTO.

Gate turn-on time for G

Gate drive can be removed once anode ch exceeds latching current..

However, some manufacturers advice that even after GTO is on, a continuous gate ch, called back porch ch E_{gb} should be applied during the entire on-period of GTO.

This is done to avoid any possibility of unwanted turn-off of the GTO.

$$T_{on} = t_d + t_r + t_p$$

Gate turn-off

Before the initiation of turn-off process, a GTO carries a steady current I_a.

The total turn-off time t_q is subdivided into three diff periods; namely the storage period (t_s), the fall period (t_f) and the tail period (t_t).

$$t_q = t_s + t_f + t_t$$

Storage time (t_s)

When the -ve gate current is applied, the turn-off process is initiated.

During the storage period, anode ch I_a & anode voltage remain constant.

Termination of the storage period is indicated by a fall in I_a & rise in V_a.

During t_s, the -ve gate ch rises to a particular value & prepares the GTO for turn-off by flushing out the stored carriers.

After t_s, I_a falls to a certain value & then abruptly changes its rate of fall.

Fall time (t_f)

The interval during which I_a falls rapidly is called t_f & is of the order of 1 μsec.

At the time $t = t_s + t_f$, there is a spike in voltage due to abrupt change in anode ckt.

Tail time (t_t)

After t_f, I_a & V_a keep moving towards their turn-off values for a time t_t (tail time).

After t_t, I_a reaches zero value & V_a undergoes a transient overshoot due to the presence of R_s, C_s & then stabilizes to its off-state value equal to the source voltage applied to the anode ckt.

Here R_s & C_s are the snubber circuit parameters.

The turn-off process is complete when tail ckt reaches zero.

Application of GTO's

Power transistor - BJT

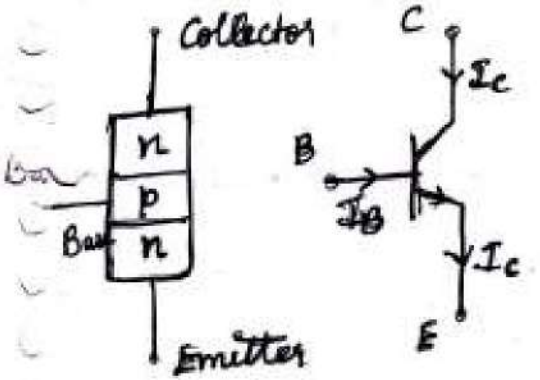
A bipolar transistor is a 3 layer, 2 jn npn (or) pnp semiconductor device.

With one p-region sandwiched by two n-regions → npn transistor.

With one n-region " " " p " → pnp "

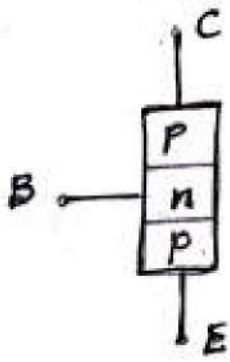
A BJT has 3 terminals named collector (C), emitter (E) & base (B).

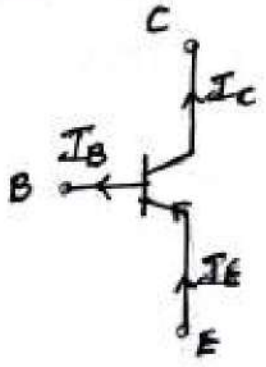
npn - transistor



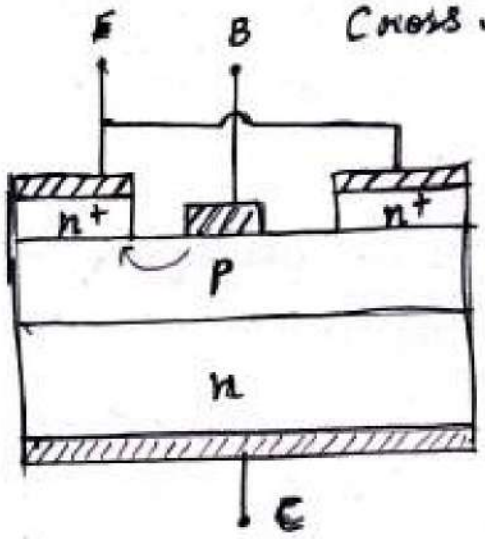
Symbol

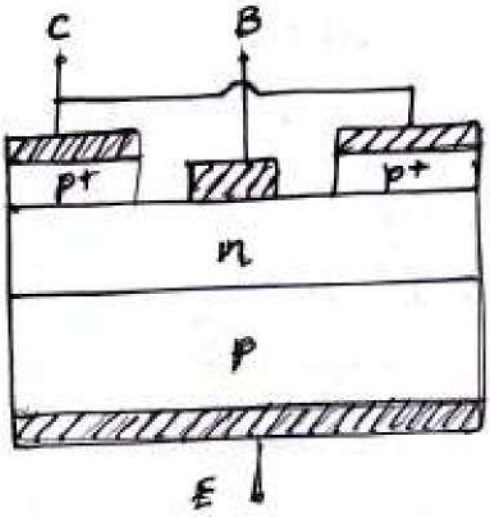
pnp - transistor





Cross section





For an NPN-type, the emitter side n-layer is made wide, the p-base is narrow, and the collector side n-layer is narrow and heavily doped.

For a PNP-type, the emitter side p-layer is made wide, the n-base is narrow, & the collector side p-layer is narrow & heavily doped.

The base & collector currents flow through two parallel path resulting in a low on-state collector-emitter resistance, $R_{CE(ON)}$.

Power transistors of npn type are easy to manufacture & are cheaper also.

Therefore, use of power n-p-n transistors is very wide in high voltage & high-current applications.

There are 3 possible ckt configurations for a transistor, CE, CC, & CB. Out of this, CE configuration is more common in switching applications.

There are 3 operating regions of a transistor: cut off, active & saturation.

Cutoff region

In this region, the transistor is off or the base current is not enough to turn it on & both junctions are reverse biased.

Active region

In this region, the transistor acts as an amplifier, where the base current is amplified by a gain & the collector-emitter voltage ↓s with the base ctg.

(Reverse Bias)

The collector-base jn is RB & base-emitter jn is FB.

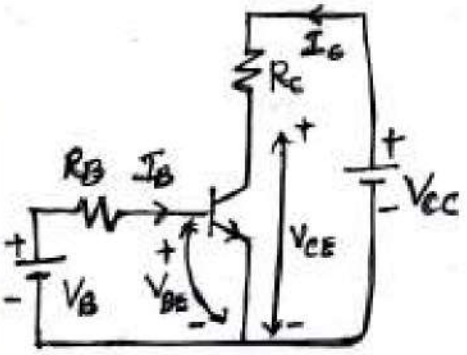
In this region, the transistor like an amplifier.

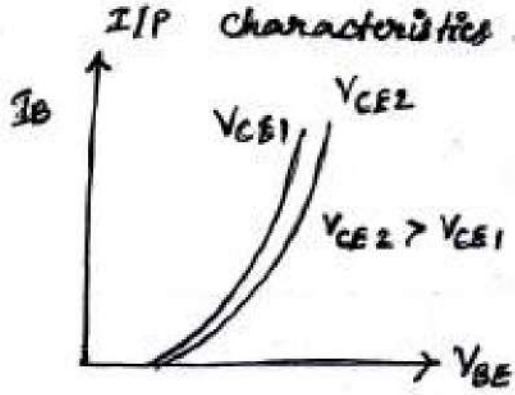
Saturation region.

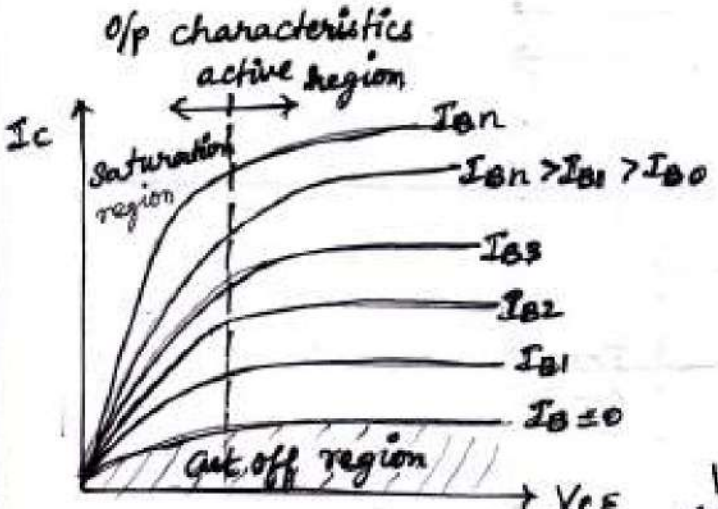
The base ctg is sufficiently high so that the collector-emitter voltage is low & the transistor acts as a switch.

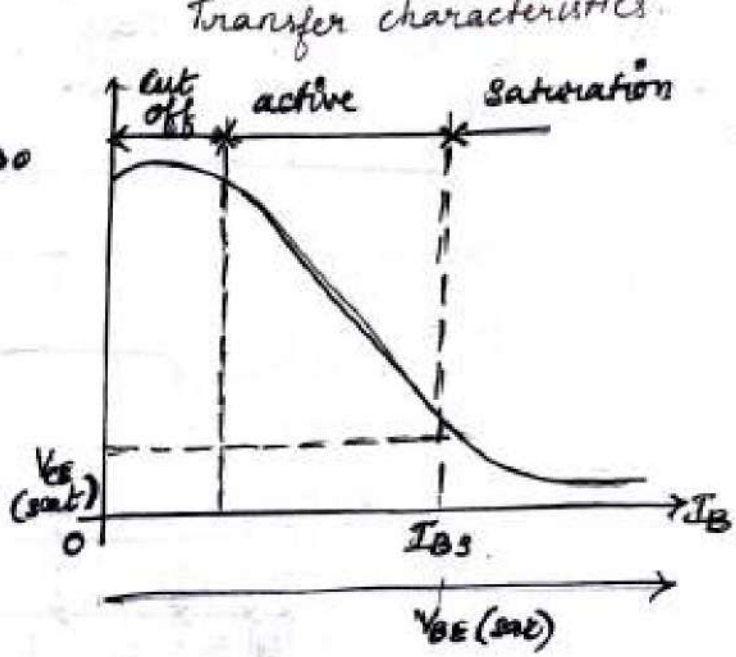
Both jn's (C-B jn & B-E jn) are fwd biased.

In this region, the transistor acts like a switch.









Current gain $\beta_f = \frac{I_C}{I_B}$

Forward current gain $\alpha = \frac{I_C}{I_E}$

Relation between α & β $\qquad \alpha = \frac{\beta}{\beta+1}$

$I_E = I_C + I_B$

$\beta = \frac{\alpha}{1-\alpha}$

÷ both by I_C

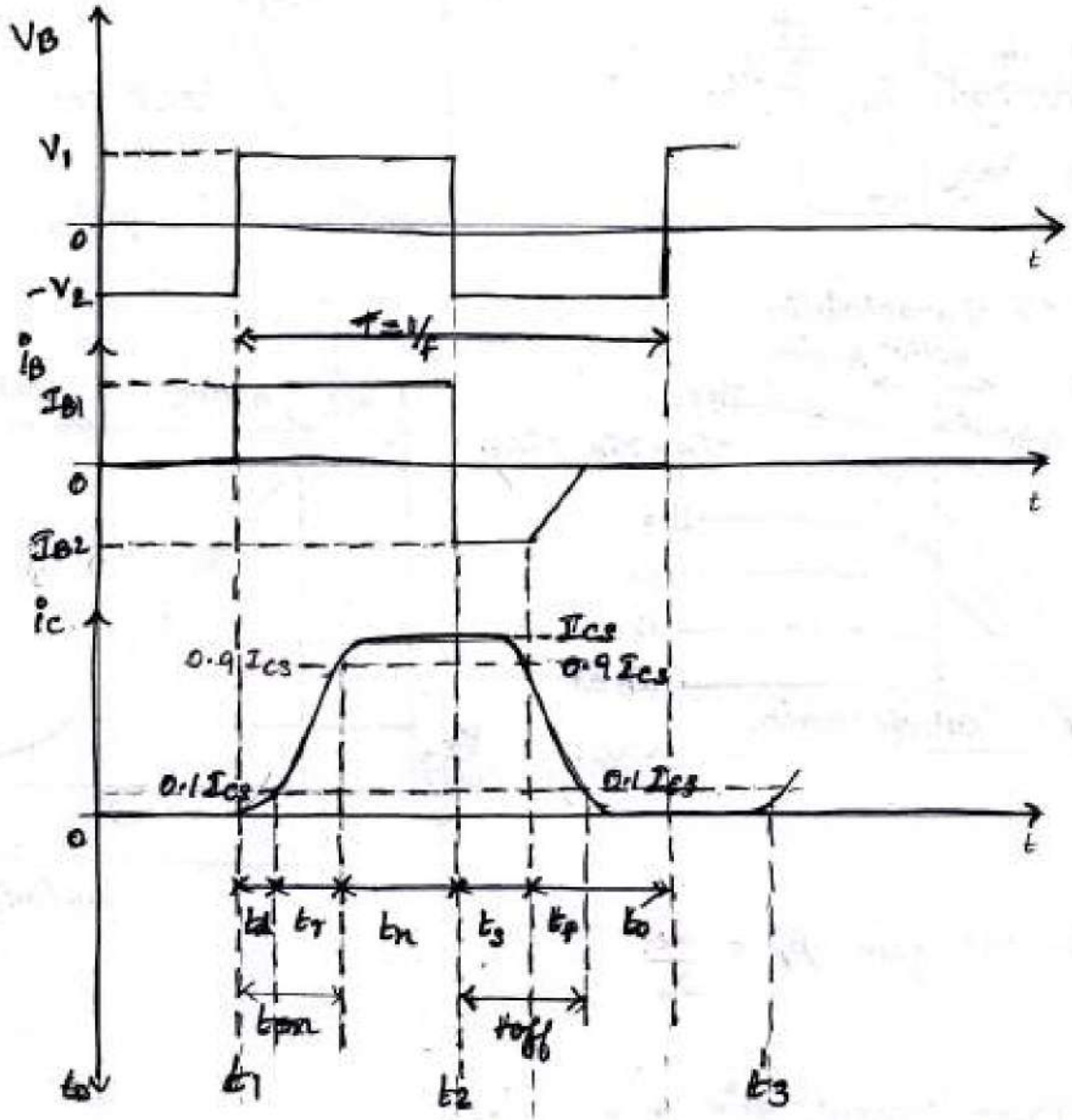
transis as switch → cutoff & Sat.

Cutoff $\quad I_C = 0 \qquad P_L = V_{CE} \times I_C = V \times 0 = 0$

Sat $\quad V_{CE} \approx 0 \qquad P_L = V_{CE} \times I_C = 0 \times I_C = 0$

$I_B = \frac{V_B - V_{BE}}{R_B}$; $I_C = \frac{V_{CC} - V_{CE}}{R_C}$.

Switching Characteristics of power BJT



When base current is applied, a transistor does not turn on instantly because of the presence of internal capacitances.

When i/p voltage V_B to base ckt is made $-V_2$ at t_0, the EB jn is RBiased, $V_{BE} = -V_2$, the transistor is off,

$i_B = I_C = 0$ & $V_{CE} = V_{CC}$.

At t_1, i/p vol V_B is made $+V_1$ & i_B rises to I_{B1}.

After t_1, V_{BE} begins to rise from $-V_2$ & i_C begins to rise from 0 & V_{CE} starts fing.

After some time delay t_d, called delay time, the i_c rises to $0.1\ I_{cs}$, V_{CE} falls from V_{cc} to $0.9\ V_{cc}$.

This delay time is required to charge the base-emitter capacitance to $V_{BE9} = 0.7V$.

Thus delay time (t_d) is defined as the time during which the i_c rises from 0 to $0.1 I_{cs}$ & V_{CE} falls from V_{cc} to $0.9 V_{cc}$.

After t_d, I_c rises from $0.1 I_{cs}$ to $0.9 I_{cs}$ & V_{ce} falls from $0.9 V_{cc}$ to $0.1 V_{cc}$ in time t_r.

The rise time t_r is defined as the time during which I_c rises from $0.1 I_{cs}$ to $0.9 V_{cc}$ & V_{CE} falls from $0.9 V_{cc}$ to $0.1 V_{cc}$.

t_r depends upon transistor jn capacitances.

Thus total turn on time $\boxed{t_{on} = t_d + t_r}$

At time t_2, i/p vol V_B to base ckt is reversed from V_1 to $-V_2$.

At the same time, base current changes from I_{B1} to $-I_{B2}$.

Negative base ctg I_{B2} removes excess carriers from the base.

The time t_s required to remove these excess carriers is called storage time (t_s) & only after t_s, I_{B2} begins to ↓ to zero.

t_s is defined as the time during which I_c falls from I_{cs} to $0.9 I_{cs}$ & V_{CB} rises from V_{CBS} to $0.1 V_{cc}$.

Fall time (t_f) is defined as the time during which I_c drops from $0.9 I_{cs}$ to $0.1 I_{cs}$ & V_{CE} rises from $0.1 V_{cc}$ to $0.9 V_{cc}$.

Thus $t_{off} = t_s + t_f$.

Gate triggering Circuit.

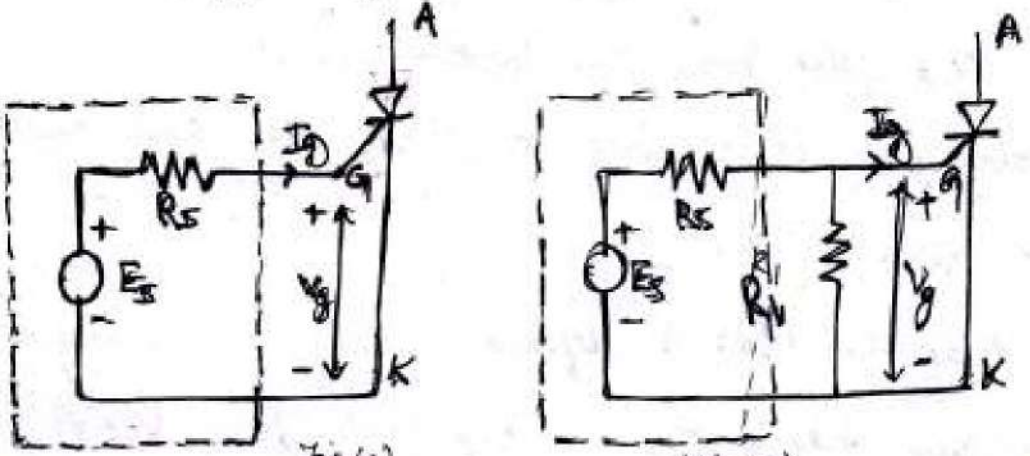


Fig (a) Fig (a) Fig (b)

This is a trigger ckt feeding power to gate-cathode ckt.

For this ckt, $E_s = V_g + I_g R_s$.

E_s - gate source voltage I_g - gate Ct.

V_g - gate-cathode voltage R_s - gate-source resistance.

The internal resistance R_s of trigger source should be such that Ct (E_s/R_s) is not harmful to the source as well as to the gate ckt when SCR is turned on.

In case R_s is low, an external resis in series with R_s must be connected.

A resistance R_1 is also connected across gate-cathode terminals.

In fig (b), so as to provide an easy path to the flow of leakage Ct obw SCR terminals.

If I_{gmn} & V_{gmn} are the min gate Ct & gate vol to turn-on SCR, then it is seen from fig (b) that Ct through R_1 is V_{gmn}/R_1 & the trigger source voltage E_s is given by

$$E_s = \left(I_{gmn} + \frac{V_{gmn}}{R_1}\right) R_s + V_{gmn}$$

For low-power ckts, it is customary to obtain the operating pt by utilizing the VI characteristics of both source & the device.

In view of this, for selecting the operating pt for the ckt fig a & b, a load line of the gate source voltage $E_s = OA$ is drawn as AD in fig c.

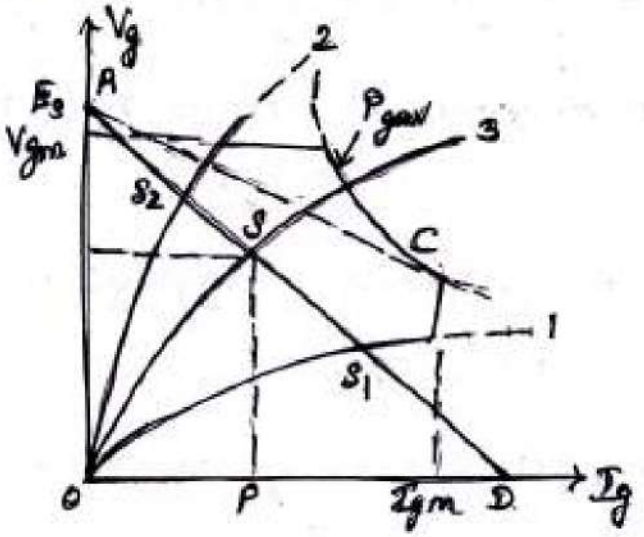


Fig C

Here OD = trigger ckt short circuit ckt = E_s/R_s.

Let us consider a thyristor whose $V_g - I_g$ characteristic is given by curve 3.

Intersection of load line AD & $V_g - I_g$ curve 3 gives the operating pt S.

Thus for SCR, gate vol = PS & gate ckt = OP.

In order to minimise turn-on time & for unreliable turn-on, the load line & hence the operating pt S, which may change from S_1 to S_2, must be as close to the P_{gav} curve as possible.

At the same time, the operating pt S must lie within the limit curves 1 & 2.

The gradient of the load line AD (= OA/OD) will give the required gate source resistance R_s.

The minimum value of gate source series resistance is obtained by drawing a line AC tangent to P_{gav} curve.

Gate drive requirements in terms of continuous dc signal can be obtained from fig b.

However, it is common to use a pulse to trigger a thyristor.

Thyristor is considered to be a charge controlled device.

Thus, higher the magnitude of gate ch^{g} pulse, lesser is the time to inject the required charge for turning-on the thyristor.

Therefore, SCR turn-on time can be reduced by using gate ch^{g} of higher magnitude.

It should be ensured that pulse width is sufficient to allow the anode ch^{g} to exceed latching ch^{g}.

In practice, gate pulse width is usually taken as equal to or greater than, SCR turn-on time.

With pulse triggering, greater amount of power dissipation can be allowed; this should, however, be less than the peak instantaneous gate power dissipation P_{gm}.

Frequency of firing for trigger pulses can be obtained by taking pulse of (i) Amplitude P_{gm} (ii) pulse width T & (iii) periodicity T_1.

$$\therefore \frac{P_{gm} T}{T_1} \geq P_{gav} \quad \text{or} \quad P_{gm} \cdot T \cdot f \geq P_{gav} \quad \text{or} \quad \frac{P_{gav}}{fT} \leq P_{gm} \longrightarrow (1)$$

$f \rightarrow \frac{1}{T_1}$ = freq of firing (Hz) T = pulse width in sec.

In the limiting case, $\frac{P_{gav}}{fT} = P_{gm}$ or $f = \frac{P_{gav}}{T \cdot P_{gm}}$

Pulsed Gate

Instead of applying a continuous (DC) gate drive, the pulsed gate drive is used.

The gate vol & ch are applied in the form of high freq pulses.

The freq of these pulses is upto 10 kHz.

Hence the width of the pulse can be upto 100 μsec.

The pulsed gate drive is applied for following reasons.

i) The SCR has small turn-on time (ie, upto 5 μsec)
Hence a pulse of gate drive is sufficient to turn on the SCR.

ii) Once SCR turns-on, there is no need of gate drive.
Hence gate drive in the form of pulses is suitable.

iii) The DC gate vol & ch ↑s losses in the SCR. Pulsed gate drive has reduced losses.

iv) The pulsed gate drive can be easily passed through isolation transformers to isolate SCR & trigger ckt.

Requirement of Gate drive.

i) The max gate power should not be exceeded by gate drive, else SCR will be damaged.

ii) The gate vol & ch should be within the limits specified by gate charac for successful turn-on.

iii) The gate drive should be preferably pulsed.

iv) The width of the pulse should be sufficient to turn-on SCR successfully

v) The gate drive should be isolated electrically from the SCR.
This avoids any damage to the trigger ckt if in case SCR is damaged

vi) The gate drive should exceed permissible -ve gate to cathode vol. otherwise SCR is damaged.

vii) The gate drive ckt should not sink ch out of the SCR after turn-on.

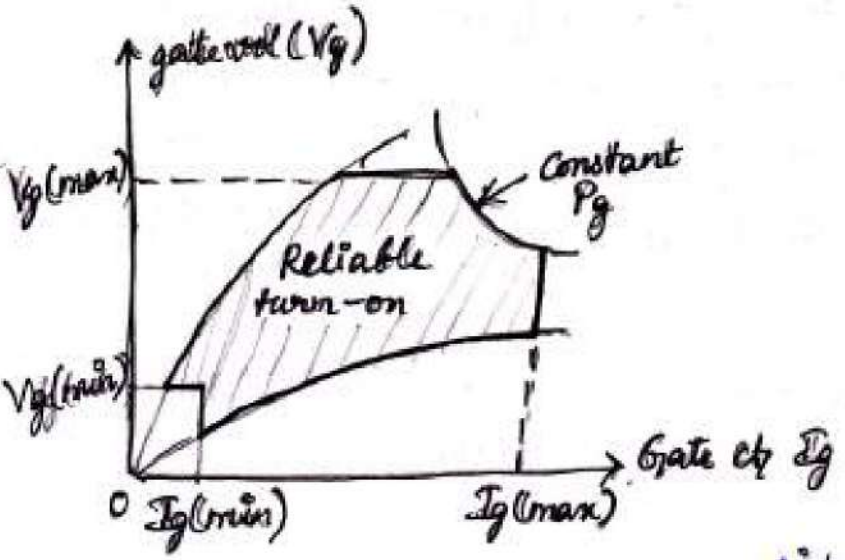
Inverter grade SCRs

The SCRs which have turn-off time less than 25 μs are called Inverter grade SCRs. Such SCRs are used in inverters, choppers etc.,

Converter grade SCRs

The SCRs having larger turn-off times ($t_q > 25\ \mu s$) are called converter grade SCRs. Such SCRs are used in controlled rectifiers, AC voltage ctrllers etc.,

SCR Gate characteristics.



The gate vol (V_g) is plotted w.r.to gate ct (I_g) in the charac.

$I_{g(max)}$ → Max gate ct that can flow through SCR without damaging it.

$V_{g(max)}$ → Max gate vol to be applied

$V_{g(min)}$ & $I_{g(min)}$ → Min gate vol & ct, below which gate ct & vol should be

$$I_{g(min)} < I_g < I_{g(max)} \text{ &}$$

$$V_{g(min)} < V_g < V_{g(max)}$$

This is the curve for constant gate power (P_g).

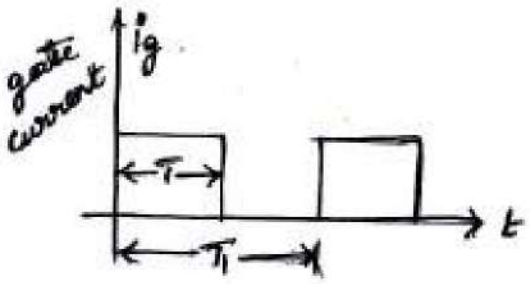
Thus for reliable turn-on, the (V_g, i_g) pt must lie in the shaded area

It turns-on SCR successfully.

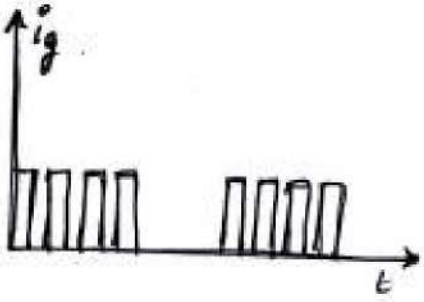
Note that any spurious vol/ct spikes at the gate must be less than $V_{g(min)}$ & $I_{g(min)}$ to avoid false triggering of SCR.

The gate shown here are for DC values of gate vol & ct.

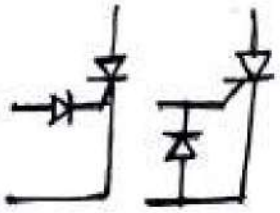
A duty cycle is defined as the ratio of pulse-on period to periodic time of pulse.



(d) Pulse gating



(e) high-frequency carrier gating of SCRs



(f) thyristor protection against reverse voltages.

In fig (d), pulse-on period is T & periodic time is T_1.

Therefore, duty cycle δ is given by, $\delta = \frac{T}{T_1} = fT$.

From ①, $\frac{P_{gav}}{\delta} \leq P_{gm}$ or $\frac{P_{gav}}{\delta} = P_{gm}$.

Sometimes, the pulses of fig (d) are modulated to generate a train of pulses as shown in fig (e).

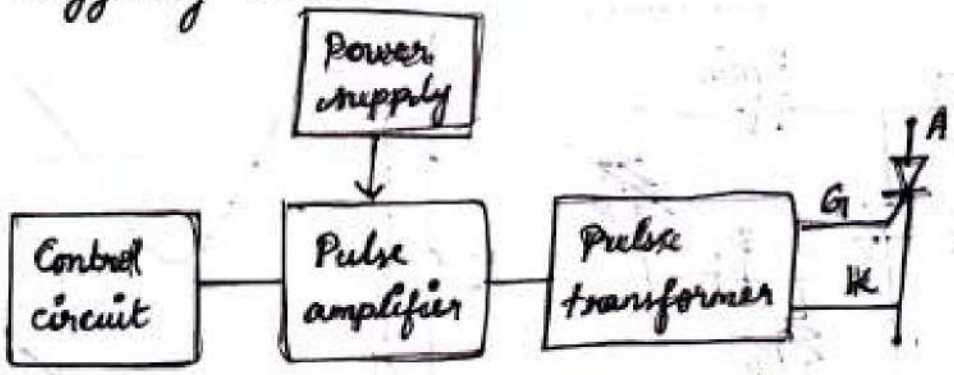
This technique of firing the thyristor is called high-frequency carries gating.

The advantages offered by this method of firing the SCRs are lower rating, reduced dimensions & therefore an overall economical design of the pulse transformer needed for isolating the low power ckt from the main power ckt.

For an SCR, V_{gm} & I_{gm} are specified separately.

The magnitude of gate vol & gate ct for triggering an SCR is inversely proportional to jn temp.

Gate triggering Circuits



The firing ckt should produce the triggering pulses for every thyristor at appropriate instants.

The triggering pulses generated by ctrl ckt need to be amplified & passed through the isolation ckt.

The triggering pulses generated by ctrl ckt have very small power.

Hence their power is fed by pulse amplifier.

The firing ckt operates at low vol levels (5 to 20 volts).

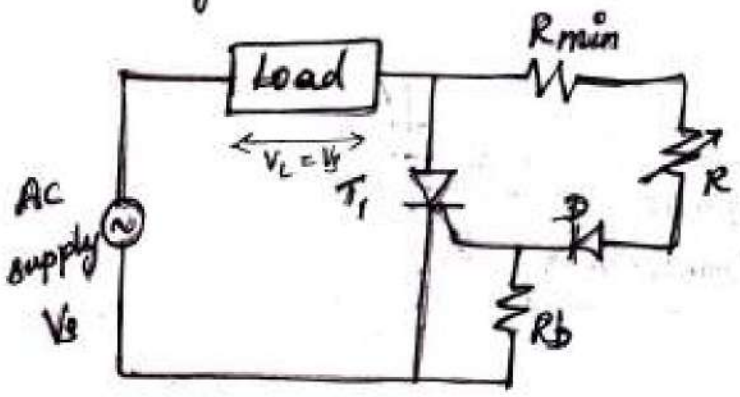
And the thyris operates at high vol levels (> 450 volts).

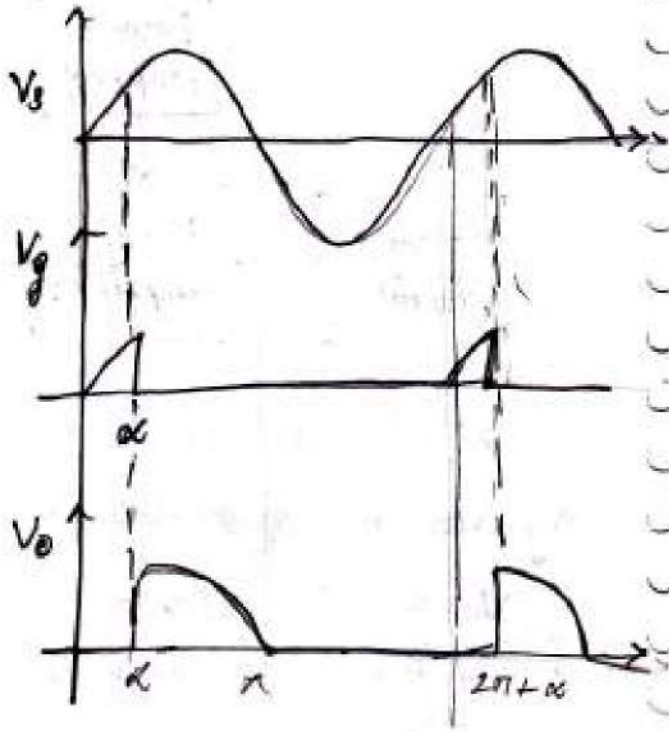
Hence there must be electrical isolation b/w firing ckt & thyristor.

↓

This is provided by the pulse transformer or opto couplers.

R - Firing ckt.





R_{min} → used to limit I_g to its max value.

$R_{min} \geq \frac{V_m}{I_g(max)}$ → peak supply volt.

R_b → stabilizing resis.

This should not exceed $V_g(min)$, else thyris will turn-on directly.

R → variable resis → to trigger T_1.

If R=0, the triggering angle is min. R ↑s, angle ↑s.

The V_{AK} & I_g are in phase.

Hence the triggering angle of T_1 cannot be delayed beyond 90°.

+ve half cycle → T_1 FB but will not conduct. D_1 also FB. ∴ I_g flowing through it will make T_1 to ON. $V_L = V_s$.

Disadv

α greatly dependent on SCR's I_g(min).

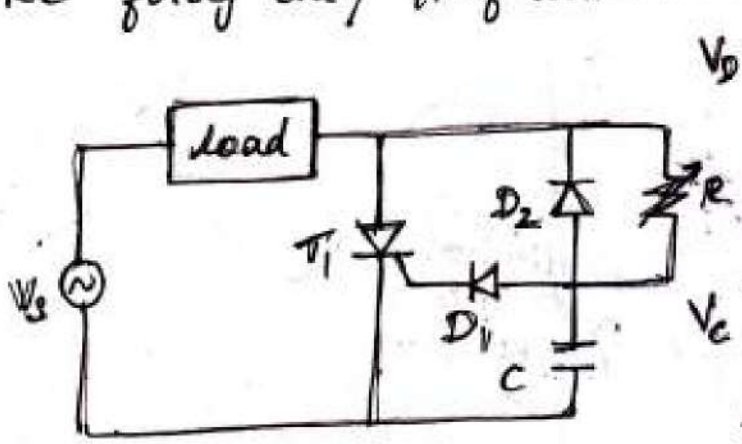
highly temp dependent.

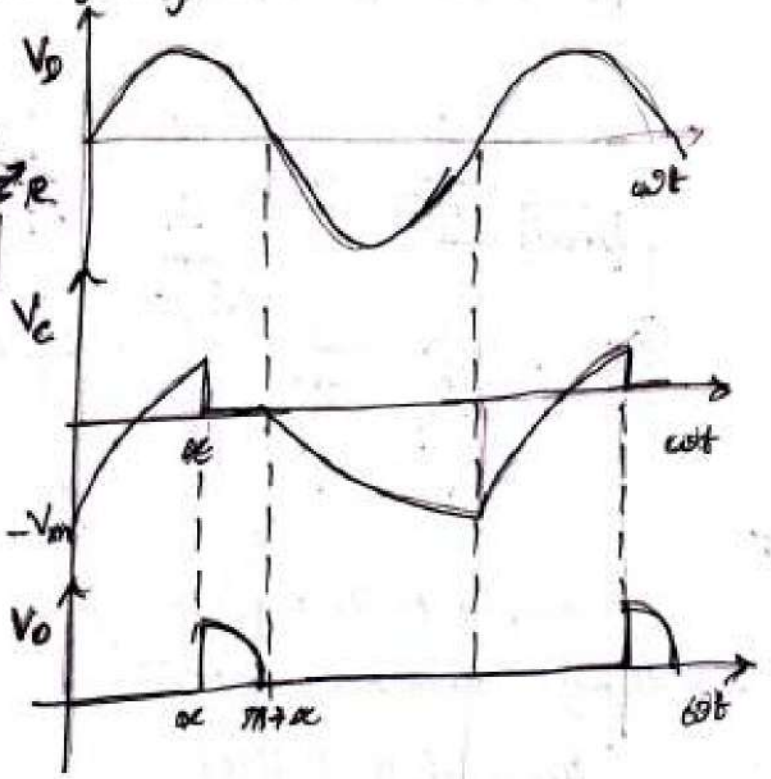
Also α can be varied only up to 90° (0 to 90° only can be varied)

During -ve half cycle → Anode to Cathode of T_1 will be RB.

∴ T_1 - off.

RC firing ckt / Half wave RC firing ckt.





i) -ve half cycle

Cap 'C' charges to $-V_m$ through D_2 to -ve supply vol.

ii) +ve half cycle

'C' discharges (ie, charges towards +ve) through R during the +ve half cycle of the supply.

The thyris T_1 triggers when 'C' charges to value $> V_g(min)$.

D_1 → prevents -ve capacitor vol appearing to gate of T_1.

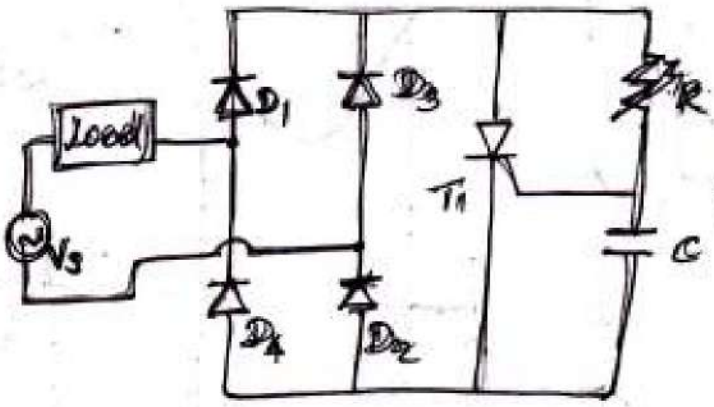
α → can be varied from 0 to 180°.

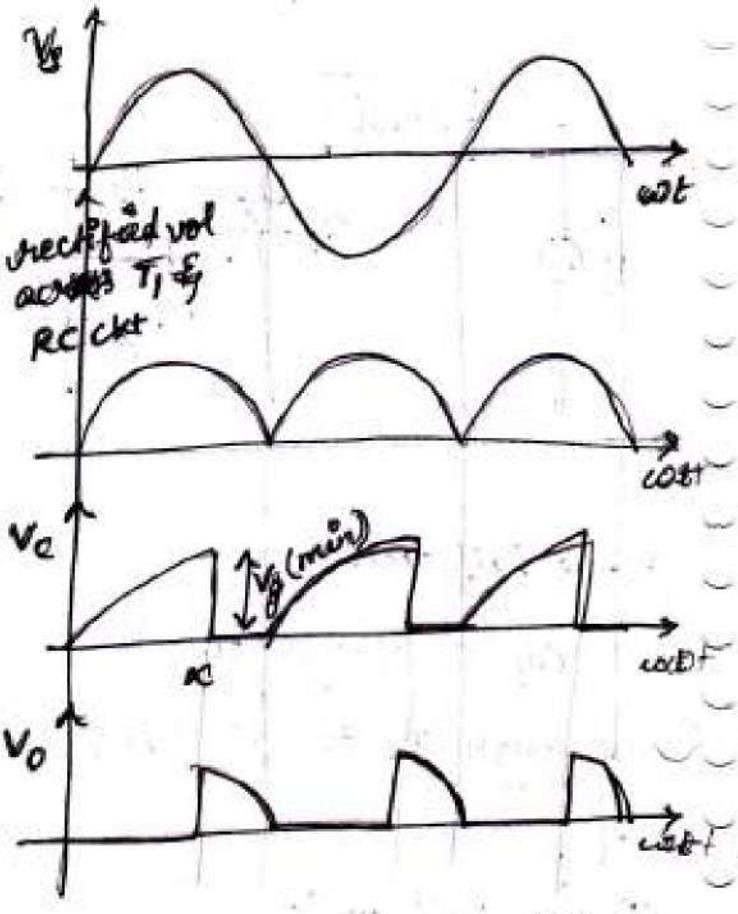
$RC \geq \frac{1.3}{2f}$ $\quad f \rightarrow$ supply freq.

Since triggering is controlled only in one half cycle of the supply, this ckt is called half wave RC firing ckt.

By varying R_1 the α can be varied from 0 to 180°

Full wave RC - firing ckt.





Supply to T_1 is given through uncontrolled rectifier.

Hence both half cycles are +ve half cycles to T_1.

The 'C' starts charging in every half cycle at the beginning.

Whenever the V_c reaches $> V_g$(min), T_1 turns-on.

Once T_1-on, V_c is clamped to zero, till next half cycle.

The 'C' again starts charging from zero.

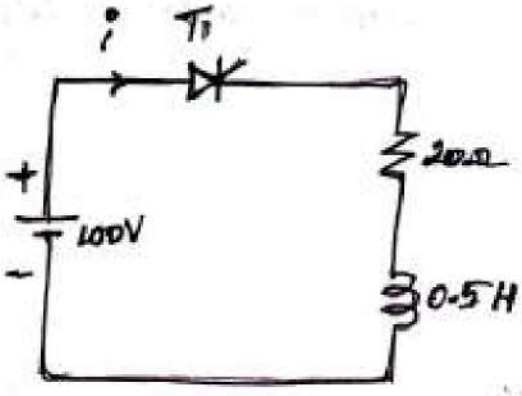
The $\alpha \rightarrow$ 0 to 180°.

triggering controlled in both cycles.

$$RC \geq \frac{0.157}{2\pi f}$$

Max firing angle.

The latching current of a thyristor ckt in fig is 50 mA. The duration of the firing pulse is 50 μs. Will the thyristor get fired?



As the SCR is triggered, the current will rise exponentially in the inductive ckt.

$$\therefore \quad i(t) = \frac{V}{R}\left(1 - e^{-t/\tau}\right)$$

where $\tau = \frac{L}{R}$

$$\tau = \frac{0.5}{20} = 0.025 \text{ sec.}$$

Given $L = 0.5$ H
$R = 20\ \Omega$
$V = 100$ V
$t = 50$ μs.

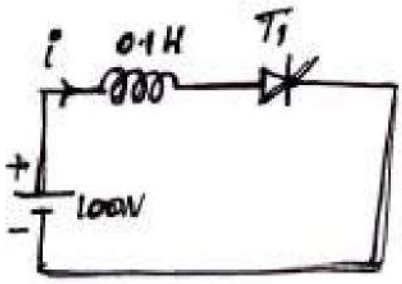
At $t = 50$ μs.

$$i(50\times10^{-6}) = \frac{100}{20}\left(1 - e^{-\left(\frac{50\times10^{-6}}{0.025}\right)}\right)$$

$$= 9.99 \text{ mA} //$$

Since the calculated circuit current value is less than the given latching ct value of the SCR, it will not get fired.

If the latching ct in the ckt shown in fig is 4 mA, obtain the minimum width of the gating pulse required to properly turn-on the SCR.



Given
$L = 0.1$ H
$V = 100$ V.
$i = 4$ mA.

$i \rightarrow$ latching ct
$t \rightarrow$ pulse width

The ckt eqn is $V = L\frac{di}{dt}$

$$dt = L\frac{di}{V}$$

Integrating on both sides, $t = \frac{L}{V} i$

$$t_{min} = \frac{0.1}{100}(4\times10^{-3})$$

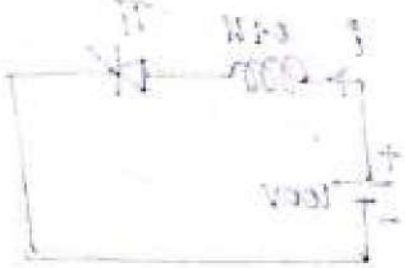
This is the min width of the gating pulse required to turn on SCR → $t_{min} = 4$ μs.

3. Compute the peak inverse voltage of thyristor connected in the three phase, 6 pulse bridge ckt having i/p voltage of 415 V. Voltage safely factor is 2.1.

W.K.T PIV $= \sqrt{2}\, V_{in}\, V_f$ $V_f \rightarrow$ Vol safely factor.

$= \sqrt{2} \times 415 \times 2.1$

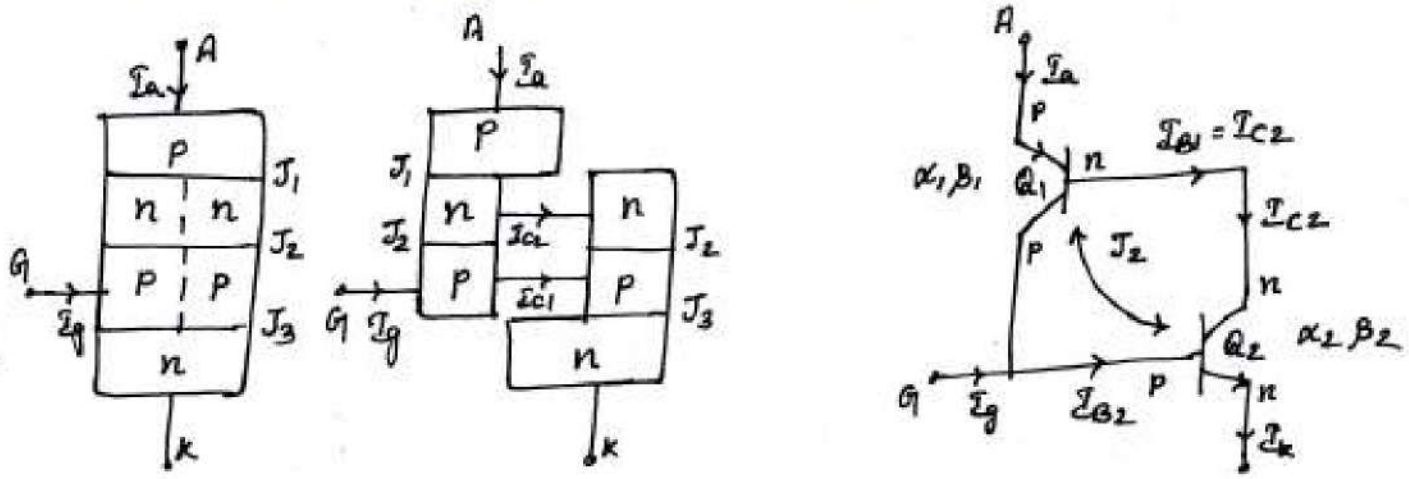
$= 1232.49$ V.



Two transistor model of a thyristor

The regenerative or latching action due to a +ve feedback can be demonstrated by using a two-transistor model of thyristor.

A thyristor can be considered as two complementary transistors, one pnp-transistor Q_1 & other npn-transistor, Q_2.



(a) Thyristor schematic diagram

(b) & (c) Two transistor model of a thyristor.

In off-state, I_C is related to I_E as,

$$I_C = \alpha I_E + I_{CBO}$$

α – Common base current gain.

I_{CBO} – Common base leakage ch.

For Q_1,

$$I_E = I_a \text{ & } I_C = I_{C1}$$

$\therefore$ For Q_1, $I_{C1} = \alpha_1 I_a + I_{CBO1}$ → (1)

α_1 = Common-base ch gain of Q_1

I_{CBO1} = Common-base leakage ch of Q_1

Wkly for Q_2, $I_{C2} = \alpha_2 I_k + I_{CBO2}$ → (2)

α_2 = Common base ch gain of Q_2

I_{CBO2} = Common base leakage ch of Q_2

I_k = Emitter ch of Q_2

① + ② ⇒ $I_a = I_{C1} + I_{C2}$

$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \rightarrow ③$

When gate sig is applied, then $I_k = I_a + I_g$. → ④

Sub ④ in ③

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

(or)

$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

For a Si transistor, ch gain α is very low at low emitter ch. with an increase in I_E, α builds up rapidly.

With $I_g = 0$ & with thyris FB, $(\alpha_1 + \alpha_2)$ is very low. Under these condns, the above eqn shows that fwd leakage ch somewhat more than $(I_{CBO1} + I_{CBO2})$ flow.

If by some means, I_E of both transistors can be fed to $\alpha_1 + \alpha_2$ to unity to make the device to turn-on.

Transistor switch:

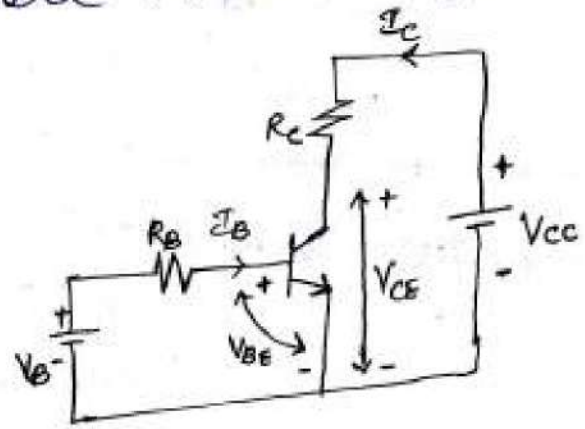
Transistor operates as a switch when it is operated in saturation (or) cut-off region & nowhere else on the load line.

In ideal cases,

transis operates at point A in sat state as closed switch with $V_{CE} = 0$ & at point B in the cutoff state as an open switch with $I_C = 0$.

In practice, for large I_B, the trans will work in sat region, at pt A with small V_{CES} → on-state vol drop.

When, the base ct is reduced to zero, the device is turned off & it operated in cut off region (operation shifts to B')



Applying KVL,

$$V_B - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_B - V_{BE}}{R_B}.$$

Also

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C.$$

But $\beta = \frac{I_C}{I_B}$ $\therefore$ $V_{CE} = V_{CC} - \beta I_B R_C.$

$$= V_{CC} - \beta \left(\frac{V_B - V_{BE}}{R_B} \right) R_C.$$

Also

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE}.$$

If V_{CES} is the collector-Emitter sat vol, then collector ckt I_{CS} is given by

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C}$$

& the corresponding minimum base current, that produces sat is

$$I_{BS} = \frac{I_{CS}}{\beta}.$$

If $I_B < I_{BS}$, then BJT operates in active region

If $I_B > I_{BS}$, then V_{CES} is almost zero $\therefore \boxed{I_{CS} = \frac{V_{CC}}{R_C}}$.

This shows that I_C at sat remains substantially const. even if I_B is ↑ed.

With $I_B > I_{BS}$, hard drive of transis is obtained. Bcoz of this on-state losses will ↑.

Over Drive Factor (ODF)

$$ODF = \frac{I_B}{I_{BS}}$$ (ODF will be as high as 4 or 5).

Forced ckt gain $\beta_f = \frac{I_{CS}}{I_B}$ < natural ckt gain β

The total power loss in two jns is

$$\boxed{P_T = V_{BE} I_B + V_{CE} I_C}$$

Under sat state, both jn's ~~of~~ Power transis is FB.

Secondary Breakdown (SB) in BJT.

- is a destructive phenomenon, results from the ckt flow to a small portion of the base, producing localized hotspots.

If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor.

The 2° breakdown is caused by thermal runaway, resulting from high ckt concentrations.

The ckt concentration may be caused by defects in the transistor structure.

The SB occurs at certain combinations of V, I & time.

Beg the time is involved, the SB is basically an energy dependent phenomenon.

Forward Biased Safe Operating Area (FBSOA)

During ton & on-state condns, the avg jn temp & SB limit the power handling capability of a transistor.

The manufacturers usually provide the FBSOA curves under specified test condns.

FBSOA indicates the $I_c - V_{CE}$ limits of the transistor & for reliable operation of the transistor must not be subjected to greater power dissipation than that shown by FBSOA curve.

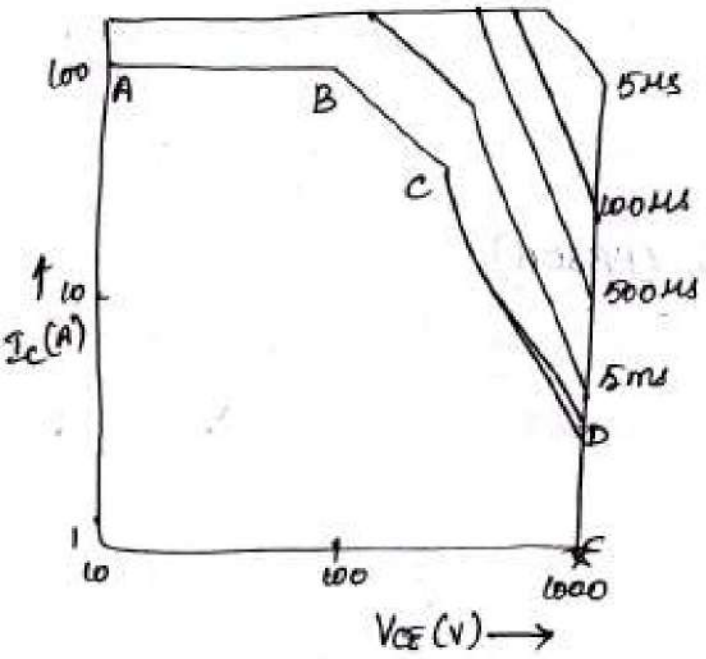
Reverse-biased Safe Operating Area (RBSOA)

During toff, a high ckt & high vol must be sustained by the transistor, in most cases with the base to emitter junction reverse biased.

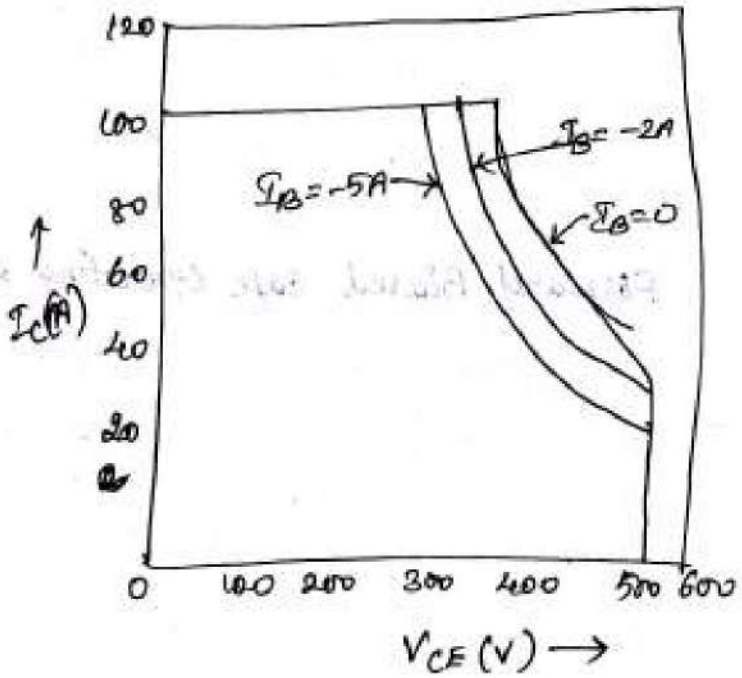
The Collector-Emitter voltage must be held to a safe level at, (or) below, a specified value of collector current.

The manufacturers provide the $I_C - V_{CE}$ limits during reverse-biased turn-off as RBSOA.

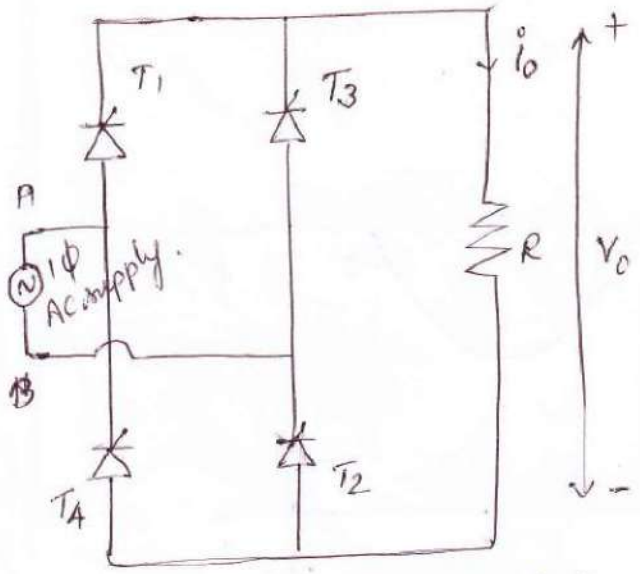
FBSOA



RBSOA.



Single phase Fully controlled bridge rectifier with R load.



1φ Fully controlled bridge rectifier consists of 4 SCRs.

Mode 1: +ve half cycle (α to π)

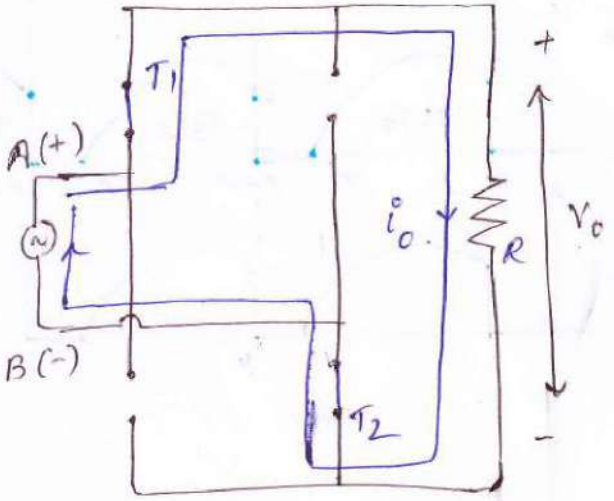
At $\omega t = \alpha$

T_1 T_2 – Forward biased.

Both triggered simultaneously.

Current flow path

$A^{(+)} \rightarrow T_1 \rightarrow R_{load} \rightarrow T_2 \rightarrow B^{(-)}$



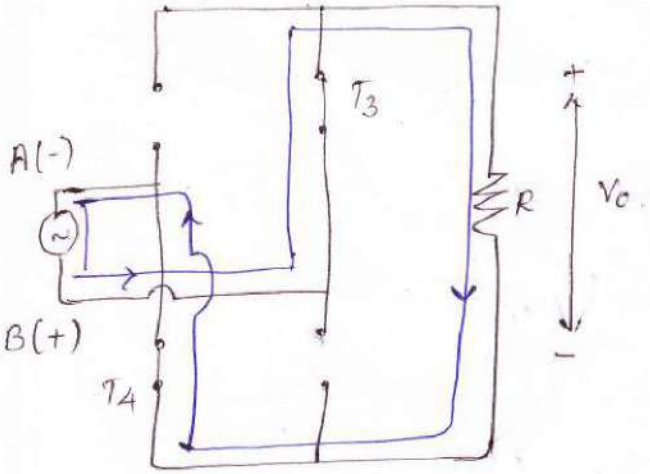
At $\omega t = \pi$

supply voltage falls to zero & the current also goes to zero.

V_o – +ve

i_o – +ve

Mode 2: -ve half cycle (~~π to~~ to 2π)



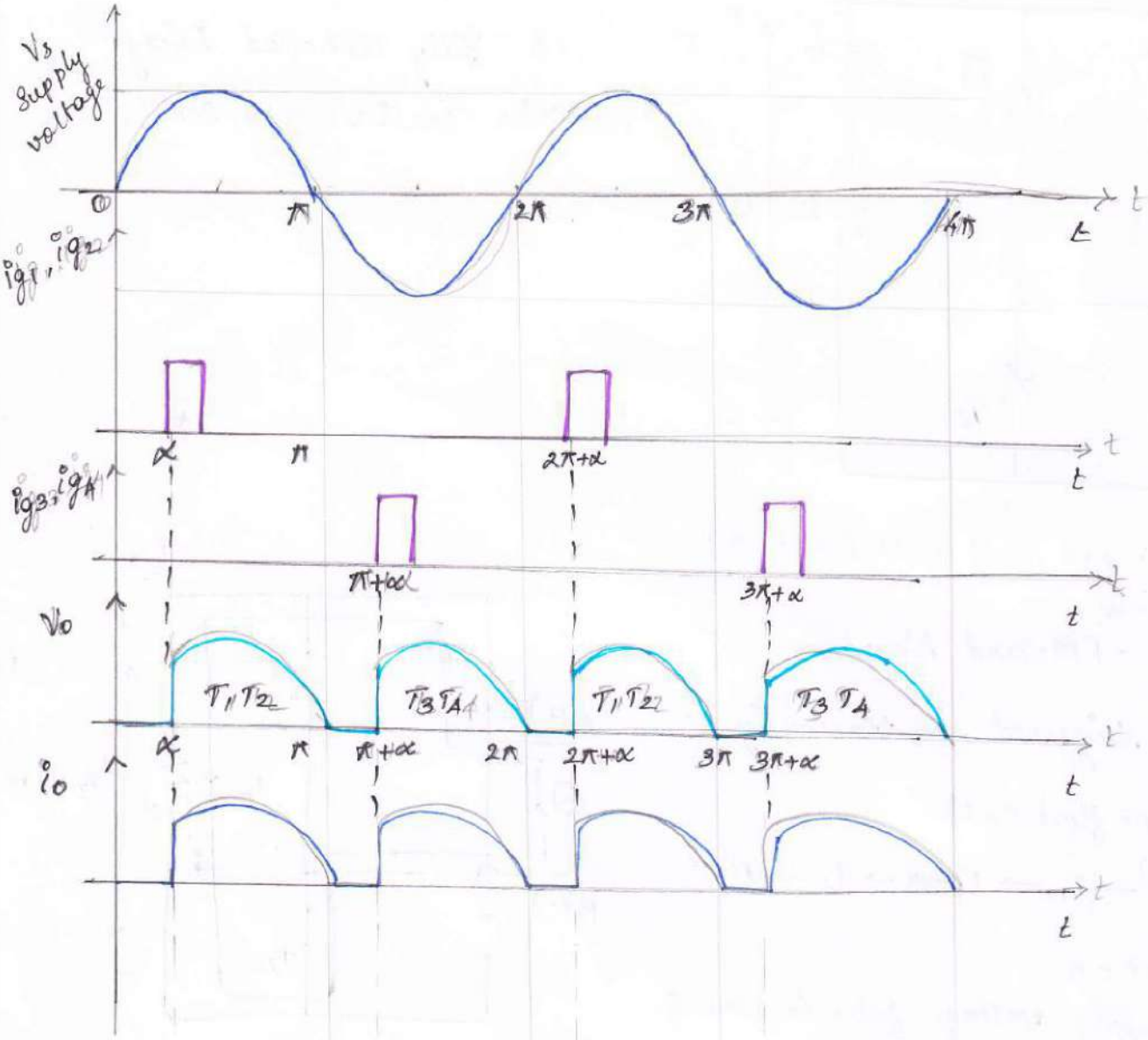
T_3 T_4 – FB.

Current flow path

$B^{(+)} \rightarrow T_3 \rightarrow R \rightarrow T_4 \rightarrow A^{(-)}$

The o/p voltage can be varied by varying the firing angle α.

As this is purely resistive load, the load current is always discontinuous.



Average o/p voltage (V_o)

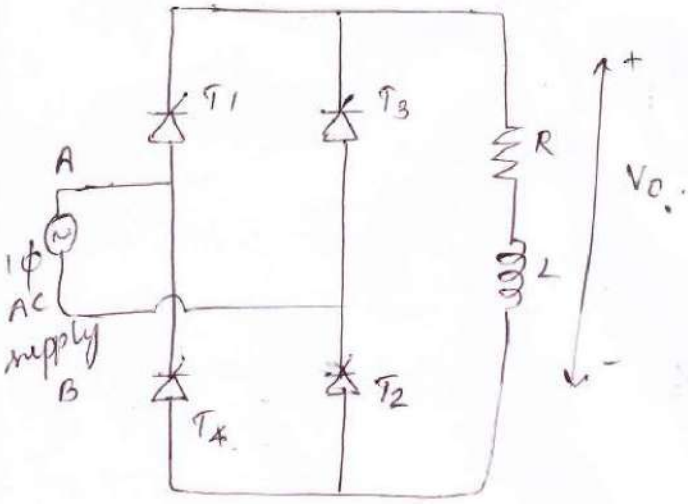
$$V_o = \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left(-\cos \omega t \right)_{\alpha}^{\pi}$$

$$= \frac{-V_m}{\pi} \left[\cos \pi - \cos \alpha \right]$$

$$\boxed{V_o = \frac{V_m}{\pi} (1 + \cos \alpha)}$$

Single phase fully controlled bridge rectifier with RL Load.



Conduction doesnot takes place until the thyristors are triggered & in order for current to flow, thyristor T_1 & T_2 must be fired together, as must T_3 & T_4 in the next half cycle from the same firing angle.

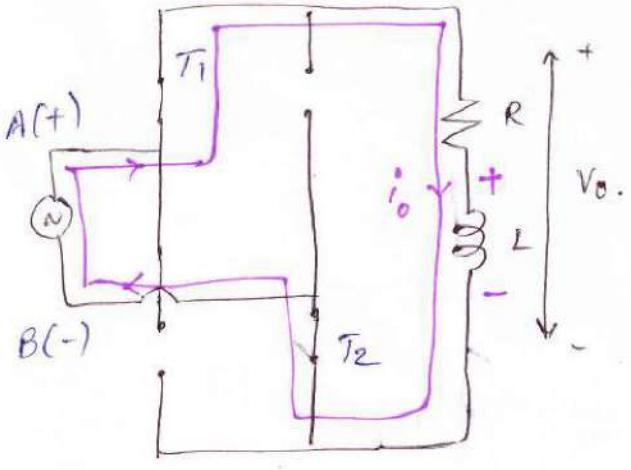
Inductance L is used to reduce the ripple

A large value of L is used for continuous steady current in the Load.

A small value of L will produce a discontinuous load current for large-firing angles.

Mode 1: α to π

T_1 T_2 – F B. (Forward Biased)



Current flow path

$A^+ \rightarrow T_1 \rightarrow RL$ load $\rightarrow T_2 \rightarrow B^-$

The Inductor (L) charges with the polarity shown in fig.

$V_o \rightarrow +ve$

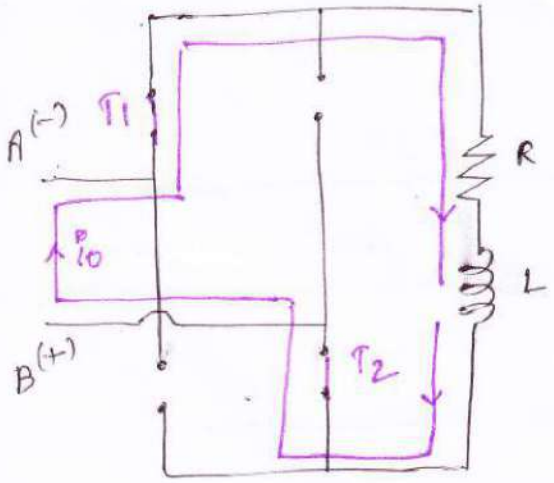
$i_o \rightarrow +ve$

Mode 2 : π to $\pi+\alpha$

Supply voltage reverses

L discharges.

Current flow path : $L \rightarrow T_2 \rightarrow B^{(+)} \rightarrow A^{(-)} \rightarrow T_1 \rightarrow RL$

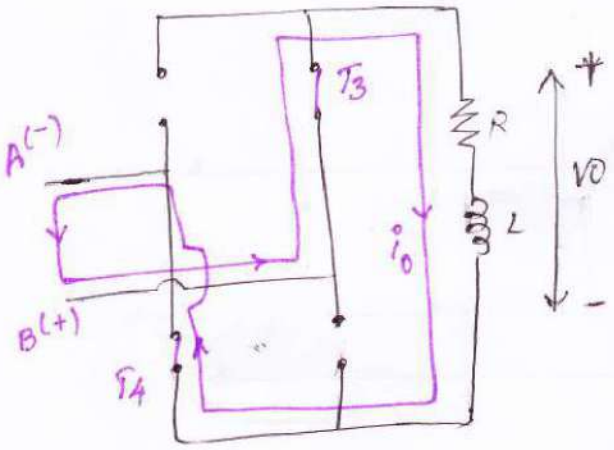


As the value of L is taken as so large, it dissipates its energy upto the time when T_3 & T_4 are triggered.

Thus V_o = -ve

i_o = +ve.

Mode 3 : $\pi + \alpha$ to 2π



T_3 T_4 - F.B

Current flow path

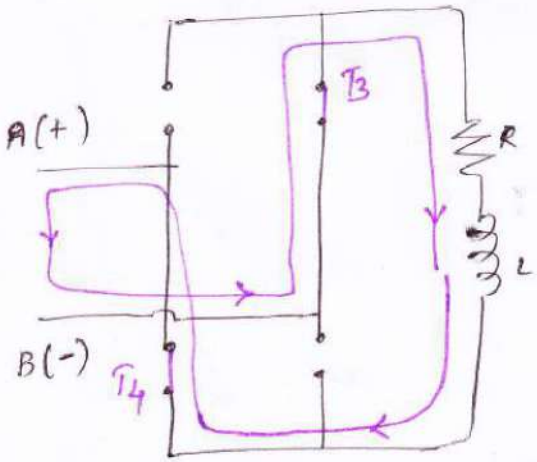
$B^{(+)} \rightarrow T_3 \rightarrow R\,L \rightarrow T_4 \rightarrow A^{(-)}$

L - charges

V_o = +ve

i_o = +ve.

Mode 4 : 2π to $2\pi + \alpha$



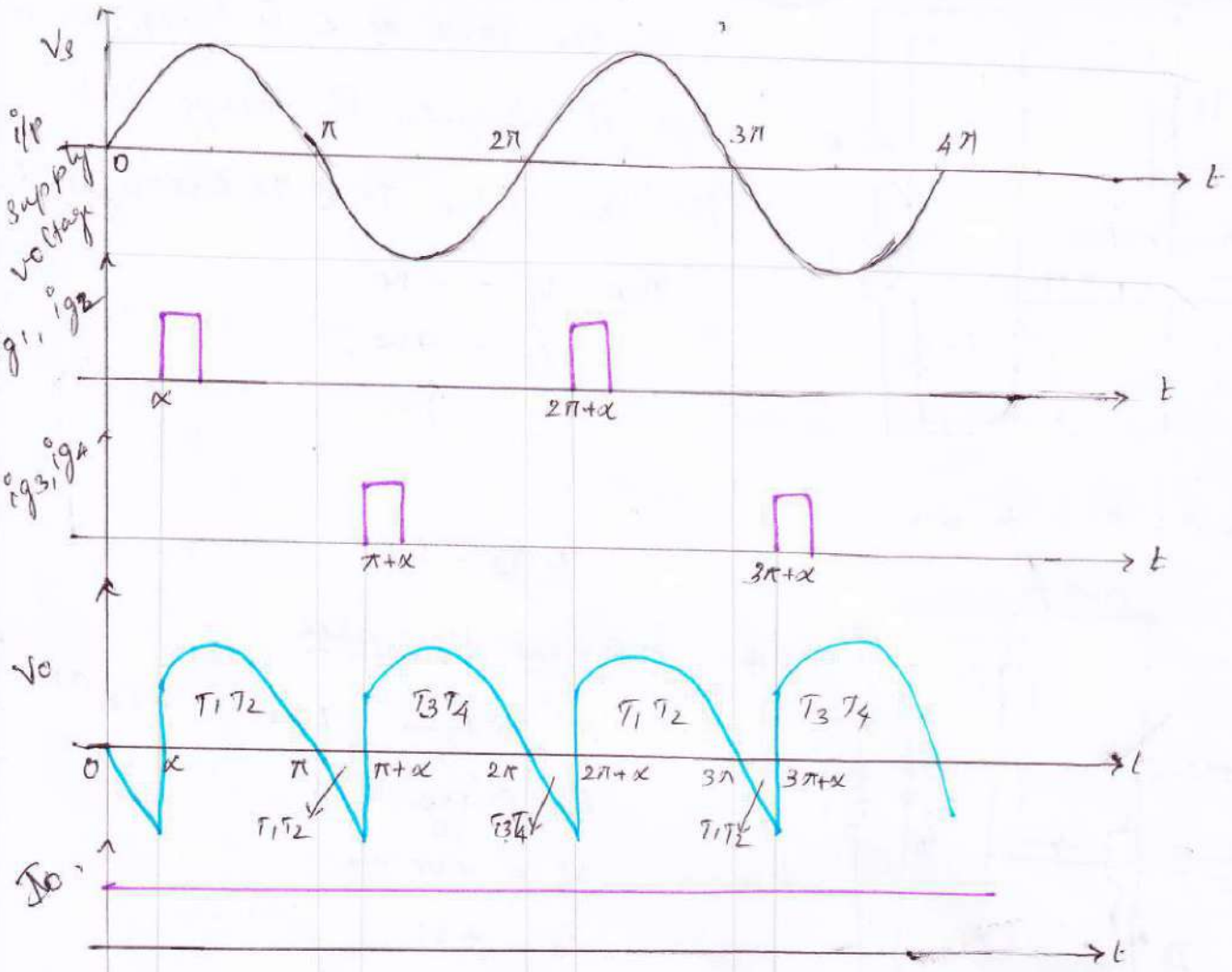
L discharges upto T_1 T_2 are fired.

Current flow path.

$RL \rightarrow T_4 \rightarrow A^{(+)} \rightarrow B^{(-)} \rightarrow T_3 \rightarrow RL$

V_o = -ve

i_o = +ve.



Average o/p voltage (V_o) (or) (V_{dc})

$$V_o = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left[-\cos\omega t \right]_{\alpha}^{\pi+\alpha}$$

$$= -\frac{V_m}{\pi} \left[\cos(\pi+\alpha) - \cos\alpha \right]$$

$$= -\frac{V_m}{\pi} \left[-\cos\alpha - \cos\alpha \right]$$

$$\boxed{V_o = \frac{2V_m}{\pi} \cos\alpha} \longrightarrow (1)$$

Rms load voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} (V_m \sin\omega t)^2 \, d\omega t \right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi} \int_{\alpha}^{\pi+\alpha} \frac{1-\cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi+\alpha} \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[(\pi+\alpha) - \frac{\sin 2(\pi+\alpha)}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi + \alpha - \frac{\sin 2\alpha}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} (\pi) \right\}^{1/2}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

As V_{dc} (or) $V_o = \frac{2V_m}{\pi} \cos\alpha$, by varying the firing angle (0° to 180°), the avg load voltage can be varied.

Here two modes of operation are possible in fully controlled bridge rectifier bcoz the power flow in the converter can be in either direction.

Conversion mode.

During the interval α to π,

Both supply voltage V_s & supply current I_s are +ve.

∴ Power flows from ac source to load.

During the interval π to $\pi+\alpha$

V_s = −ve but I_s = +ve.

The load therefore returns some of its energy to the supply system.

But the net power flows from ac source to dc load.

Thus from equation (1), for $\alpha < 90^\circ$, the voltage at the load terminals is +ve.

∴ Power flows from ac side to dc side & the converter operates as a rectifier.

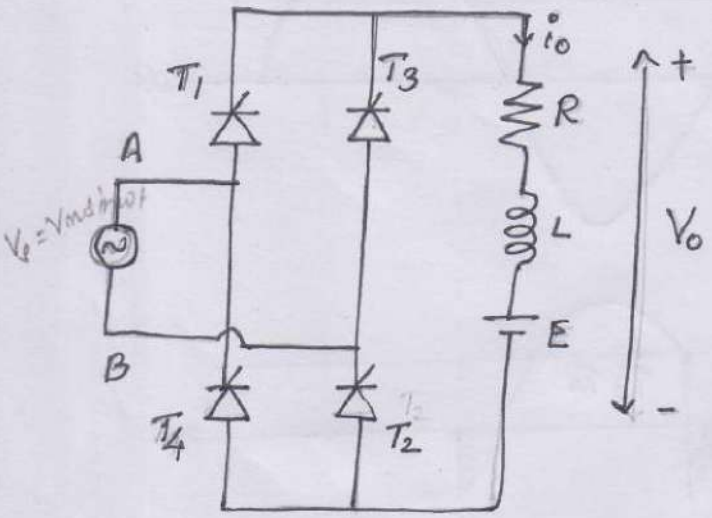
Inversion mode.

If $\alpha > 90^\circ$, the voltage at the load terminals is -ve.

Therefore, the power flows from dc side to ac side & hence the converter operates as a line commutated inverter.

In this mode power flows from load to source.

Fully Controlled Bridge Rectifier [RLE load]



Assume load inductance is high.

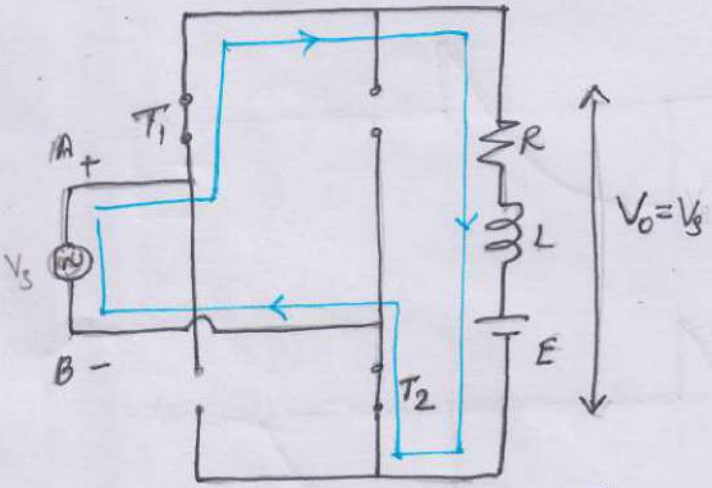
Due to this, load current is continuous and ripple free.

The load is assumed to be of RLE type, where E is the load circuit emf.

Voltage E may be due to a battery in the load circuit (or) may be generated emf of a dc motor.

Mode 1: (α to π) +ve half cycle

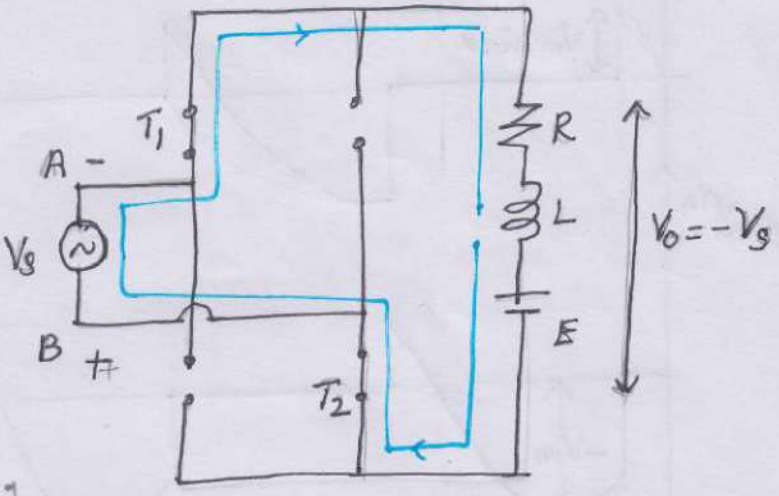
T_1 & T_2 will turn on only if $V_s > E$



$A \rightarrow T_1 \rightarrow RLE \rightarrow T_2 \rightarrow B$, V_s - +ve i_s - +ve

Power → source to load

Mode 2: (π to ~~$\pi+\alpha$~~)



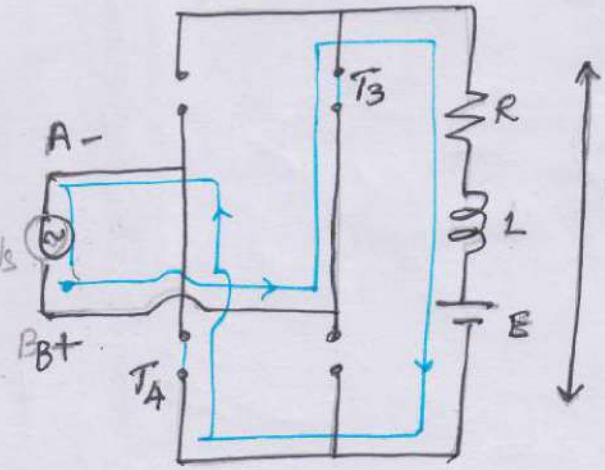
$RLE \rightarrow T_2 \rightarrow B \rightarrow A \rightarrow T_1 \rightarrow RLE$

V_s - -ve i_s - +ve

Power flows from load to source

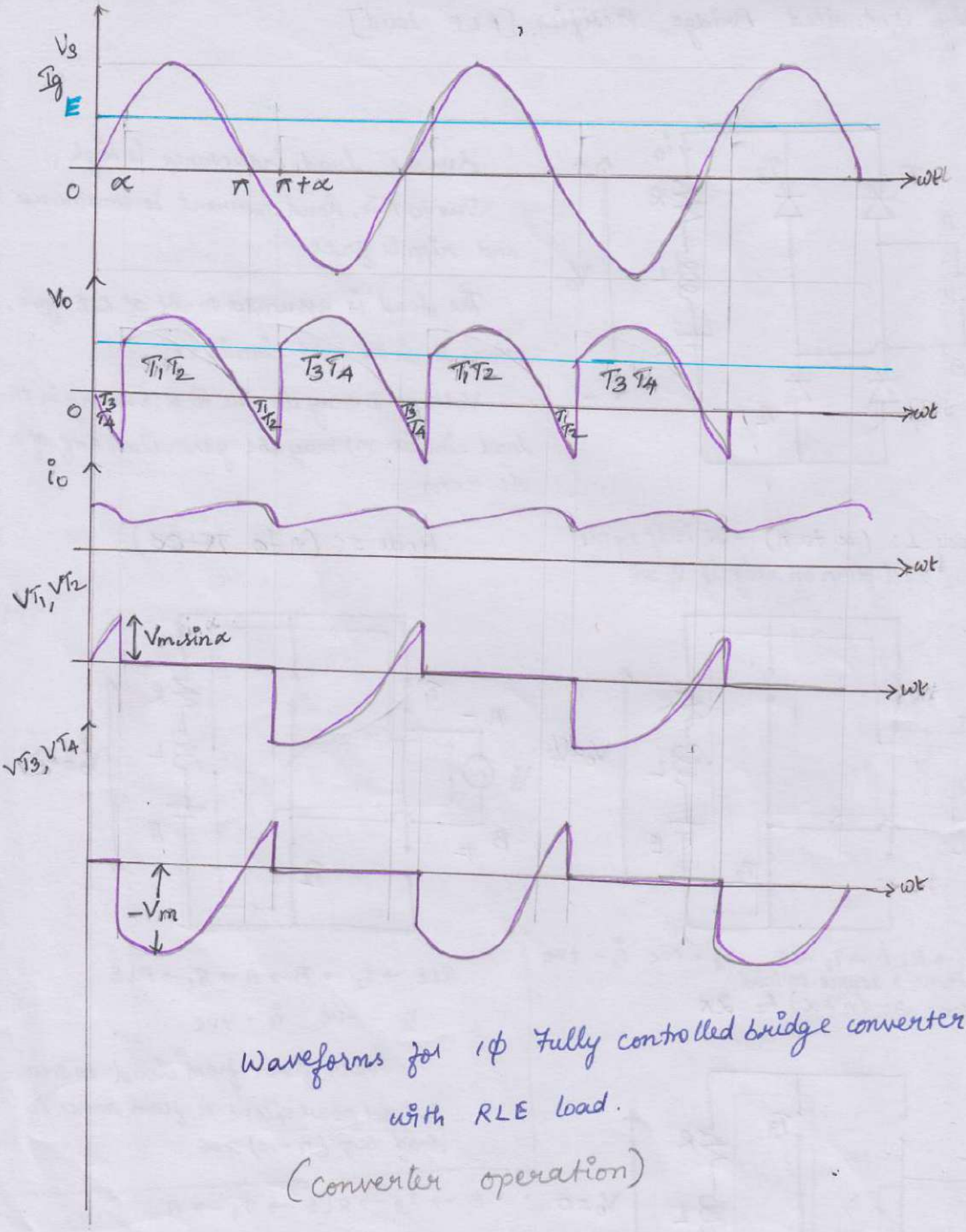
But net power flow is from source to load bcz $(\pi - \alpha) > \alpha$.

Mode 3: $(\pi+\alpha)$ to 2π



$B \rightarrow T_3 \rightarrow RLE \rightarrow T_4 \rightarrow A$.

$\Rightarrow$ Power → source to load.



Waveforms for 1ϕ fully controlled bridge converter with RLE load.

(converter operation)

Average dc output voltage

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi+\alpha}$$

$$= -\frac{V_m}{\pi}\left[\cos(\pi+\alpha) - \cos\alpha\right]$$

$$= -\frac{V_m}{\pi}\left[-\cos\alpha - \cos\alpha\right]$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}\cos\alpha}$$

Average load current

$$I_{dc} = \frac{V_{dc} - E}{R}$$

RMS o/p voltage V_{rms}

$$V_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m^2 \sin^2\omega t \, d\omega t\right]^{1/2}$$

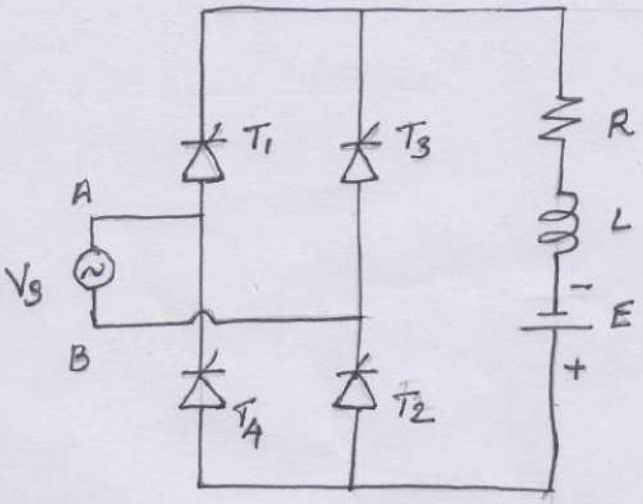
$$= \left[\frac{V_m^2}{\pi}\int_{\alpha}^{\pi+\alpha} \frac{1-\cos 2\omega t}{2} \, d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi+\alpha}\right]^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\pi+\alpha - \frac{\sin 2(\pi+\alpha)}{2} - \alpha + \frac{\sin 2\alpha}{2}\right]\right\}^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\pi - \frac{\sin 2\alpha}{2} + \frac{\sin 2\alpha}{2}\right]\right\}^{1/2} = \left(\frac{V_m^2}{2}\right)^{1/2} = \frac{V_m}{\sqrt{2}}$$

Inverter mode of operation of 1φ fully controlled bridge conv (RLE load)



For $\alpha > 90^\circ$, o/p vol V_o is negative.

If the load circuit emf E is reversed & with $\alpha > 90^\circ$, then this dc source E will feed power back to ac source.

This operation of full converter with $\alpha > 90^\circ$ is known as inverter operation.

The full conv with firing angle delay greater than 90° is called line-commutated inverter.

Mode 1 : α to π

V_s - +ve

i_s - +ve

Power → ac source to dc source.

Mode 2 : π to $\pi + \alpha$

V_s - +ve

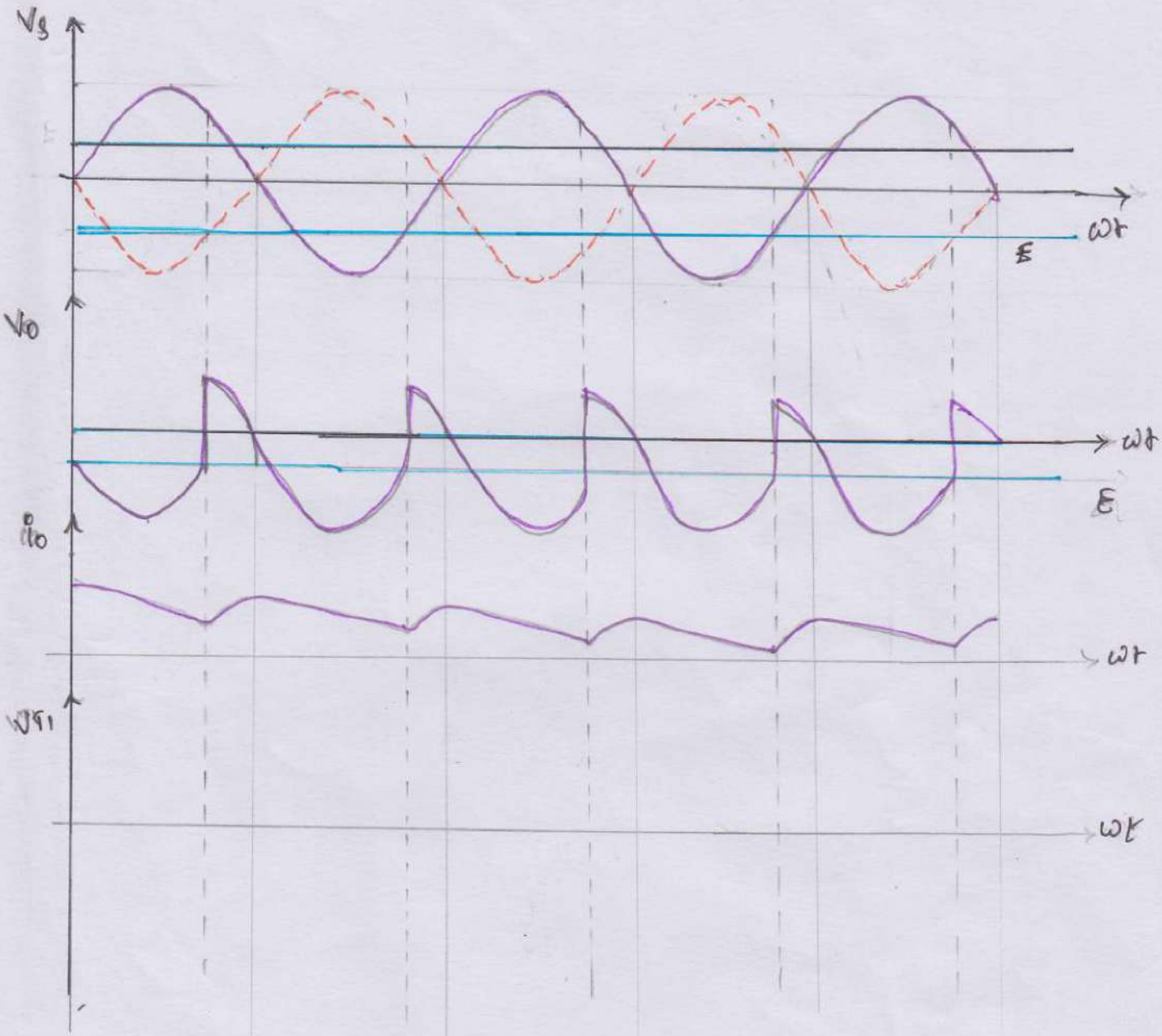
i_s - -ve

Power → dc to ac source.

* but net power flow is from dc to ac.

* In converter operation, V_o should be greater than E.
* For inverter " $E > V_o$, then only the power would flow from dc source to ac supply system.

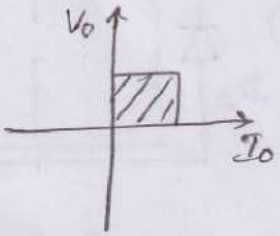
Waveform for 1ϕ fully controlled bridge converter with RLE load (Inverter operation)



Single phase semiconverter (Half controlled bridge Rectifier) / 1 Quad Converter.

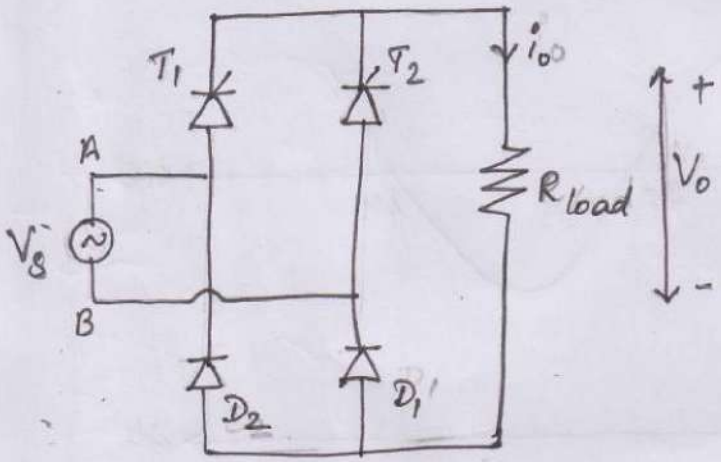
Semiconverter uses a mixture of diodes & thyristors. Hence there will be a limited control over the level of dc o/p voltage.

The o/p voltage and current is always positive. Thus it is called as 1 quadrant converter.



Semiconverter — Symmetrical configuration
Asymmetrical "

1φ Half controlled bridge rectifier with R load (Symmetrical Configuration)



Circuit consists of the combinations of thyristors & diodes.

Single gate pulse is enough to trigger the SCR's, since the cathodes of 2 SCRs are at the same potential.

$V_s = V_m \sin \omega t$

Mode 1 : +ve half cycle (α to π)

T_1 D_1 — FB

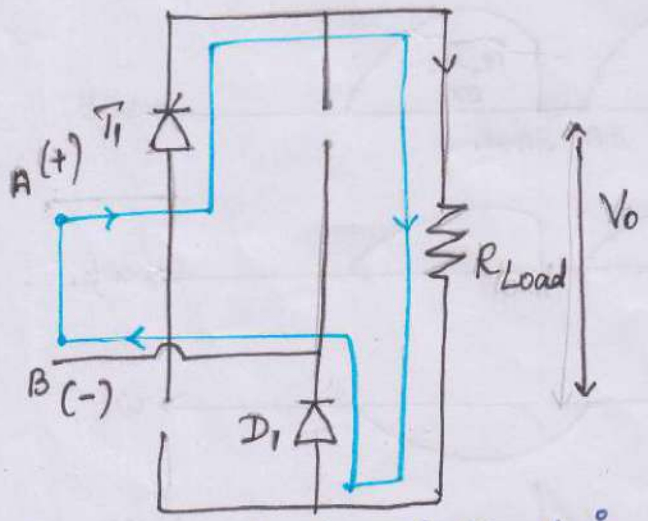
$(A^+) \rightarrow T_1 \rightarrow R \rightarrow D_1 \rightarrow (B^-)$

↓

Path of current flow.

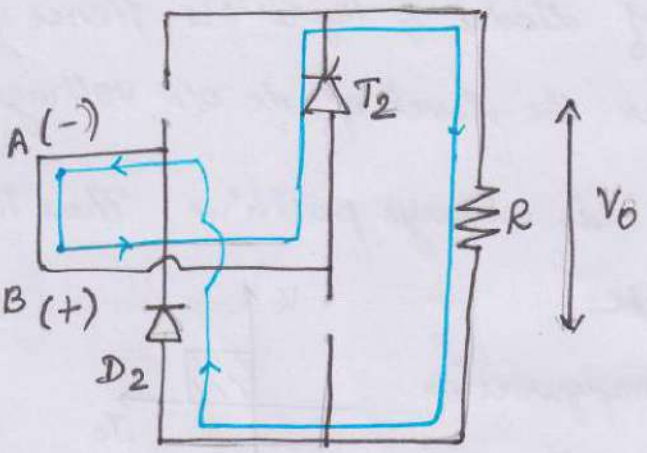
V_o - +ve

i_o - +ve



At $\omega t = \pi$, load voltage V_o & i_o reaches to zero, then T_1 & D_1 comes to off state due to natural commutation.

Mode 2 : $(\pi + \alpha)$ to 2π



T_2 D_2 – conducts

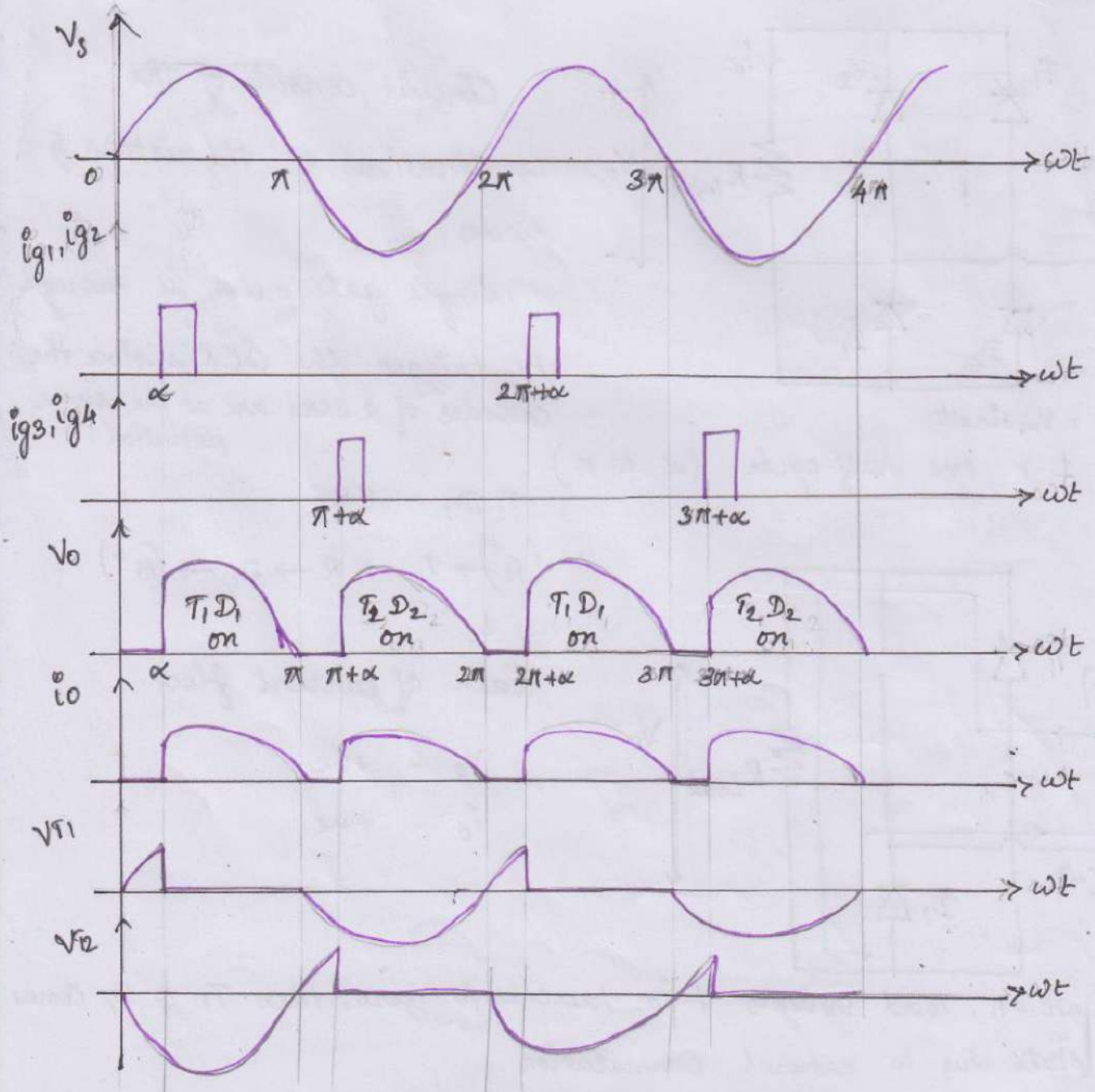
Path of load current

$B \rightarrow T_2 \rightarrow R \rightarrow D_2 \rightarrow A$

V_o - +ve

i_o - +ve

At 2π, T_2 & D_2 comes to off state due to natural commutation.



Average DC voltage : (V_{dc})

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi}$$

$$= -\frac{V_m}{\pi}\left[\cos\pi - \cos\alpha\right]$$

$$= -\frac{V_m}{\pi}\left[-1 - \cos\alpha\right]$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}(1+\cos\alpha)}$$

Average load current (I_{dc})

$$I_{dc} = \frac{V_{dc}}{R}$$

$$\boxed{I_{dc} = \frac{V_m}{\pi R}(1+\cos\alpha)}$$

RMS load voltage $V_{rms} = \left(\frac{1}{\pi}\int_{\alpha}^{\pi} V_s^2 \, d\omega t\right)^{1/2}$

$$V_{rms} = \left(\frac{V_m}{\pi}\int_{\alpha}^{\pi}(\sin\omega t)\, d\omega t\right)$$

$$= \left\{\frac{V_m^2}{\pi}\int_{\alpha}^{\pi}\sin^2\omega t \, d\omega t\right\}^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\int_{\alpha}^{\pi}\frac{1-\cos 2\omega t}{2}\, d\omega t\right]^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi}\right\}^{1/2}$$

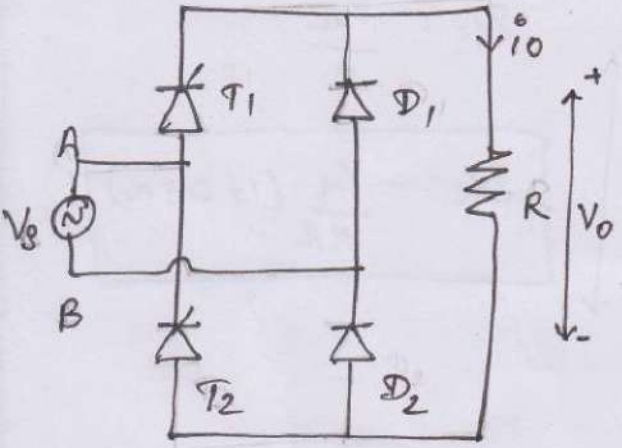
$$= \left\{\frac{V_m^2}{2\pi}\left[\pi - \frac{\sin 2\pi}{2} - \alpha + \frac{\sin 2\alpha}{2}\right]\right\}^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right\}^{1/2} = \frac{V_m}{\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}$$

$$V_s = V_m \sin\omega t.$$

$$I_{rms} = \frac{V_{rms}}{R}.$$

Half Controlled bridge rectifier with R load (Asymmetrical configuration)



In Asymmetrical configuration, separate-triggering circuits are to be used.

So that the conduction period of the thyristors will be different from diode conduction period

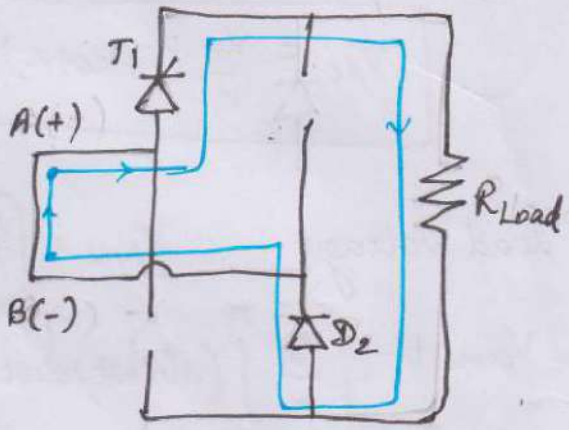
Mode 1: α to π

T_1 D_2 conducts

$A(+) \rightarrow T_1 \rightarrow R \rightarrow D_2 \rightarrow B(-)$

V_o - +ve i_o - -ve

Mode 1



Mode 2: $\pi+\alpha$ to 2π

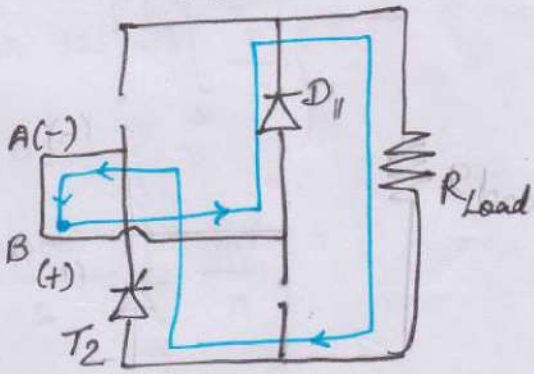
T_2 D_1 conducts

$B(+) \rightarrow D_1 \rightarrow R \rightarrow T_2 \rightarrow A(-)$

V_o - +ve

i_o - +ve

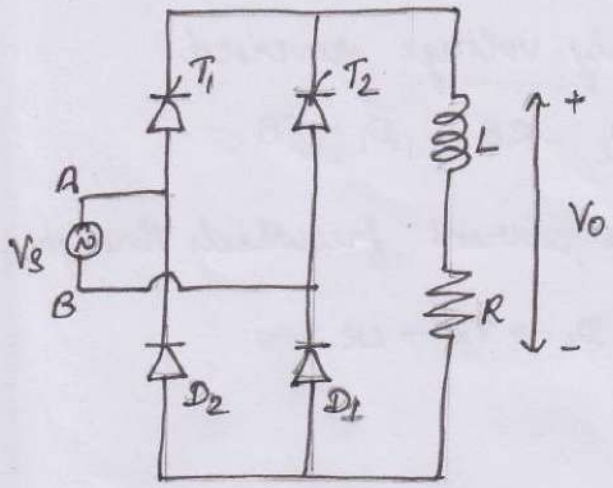
Mode 2



Average dc load voltage, Average load current, RMS voltage is similar to symmetrical configuration of semiconverter.

Waveform also like, but the conducting devices during mode 1 ($T_1 D_2$) & mode 2 ($T_2 D_1$) only changes.

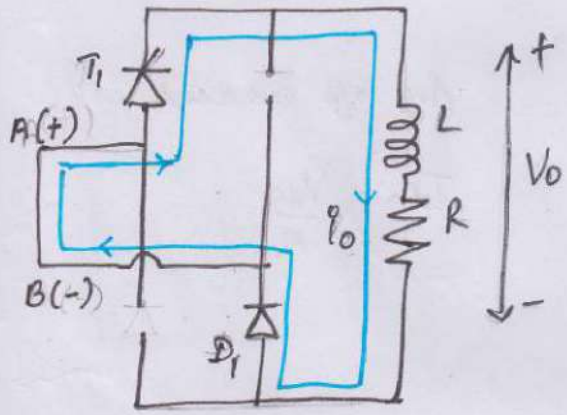
1φ Half controlled bridge converter with RL Load (Symmetrical Configuration)



The value of inductance 'L' is assumed to be large. so that the current waveform of load will be continuous.

Hence load current I_o is taken to be constant.

Mode 1 : α to π



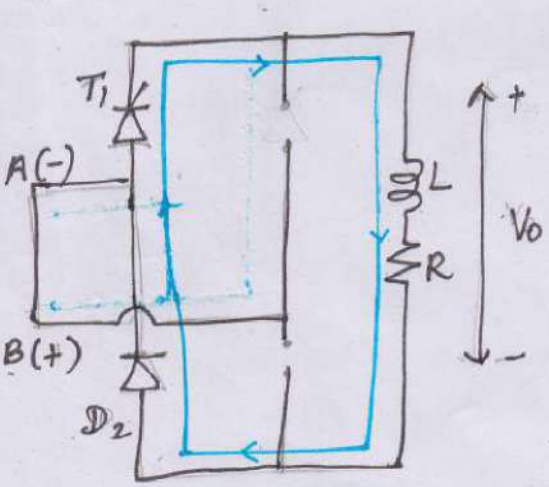
T_1 D_1 – FB

$A^{(+)} \rightarrow T_1 \rightarrow LR \rightarrow D_1 \rightarrow B^{(-)}$

V_o - +ve

i_o - +ve

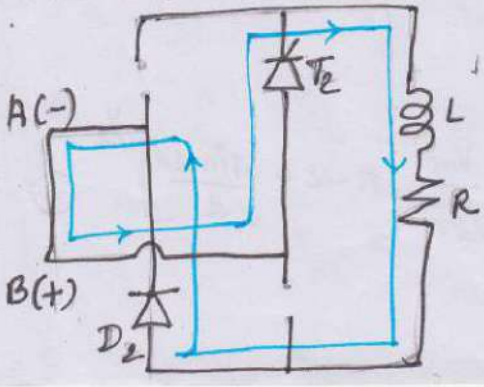
Mode 2 : π to $\pi + \alpha$



Supply voltage reverse biases D_1 & turns it off. D_2 – FB

Thus the load ckt freewheels through $LR \rightarrow D_2 \rightarrow T_1 \rightarrow LR$

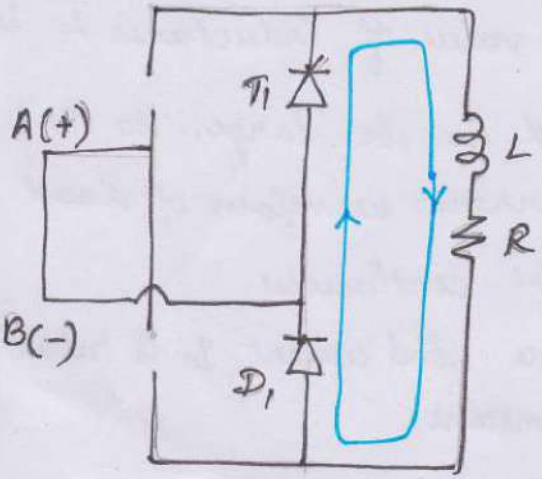
mode 3 : $(\pi + \alpha)$ to 2π



T_2 D_2 – FB

$B^{(+)} \rightarrow T_2 \rightarrow LR \rightarrow D_2 \rightarrow A^{(-)}$

Mode 4 : 2π to $(2\pi + \alpha)$



Supply voltage reversed.

So D_2 - RB . D_1 - FB .

Load current freewheels through

$LR \rightarrow D_1 \rightarrow T_1 \rightarrow LR$

Advantage : No need of additional Free Wheeling Diode.

Average dc o/p voltage

$$V_{dc} \text{ (or) } V_o = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi}$$

$$= -\frac{V_m}{\pi}\left[\cos\pi - \cos\alpha\right]$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}(1+\cos\alpha)}$$

Avg o/p current

$$I_{dc} = \frac{V_{dc}}{R}$$

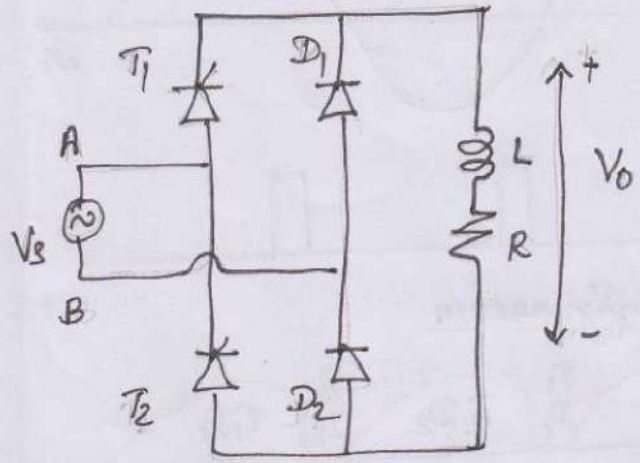
Average RMS o/p voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi}(V_m \sin\omega t)^2 d\omega t\right]^{1/2}$$

$$= \left\{\frac{V_m^2}{\pi}\int_{\alpha}^{\pi}\frac{1-\cos 2\omega t}{2}\, d\omega t\right\}^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi}\right\}^{1/2} = \frac{V_m}{\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}$$

1φ Half controlled bridge rectifier with RL Load (Asymmetrical configuration)

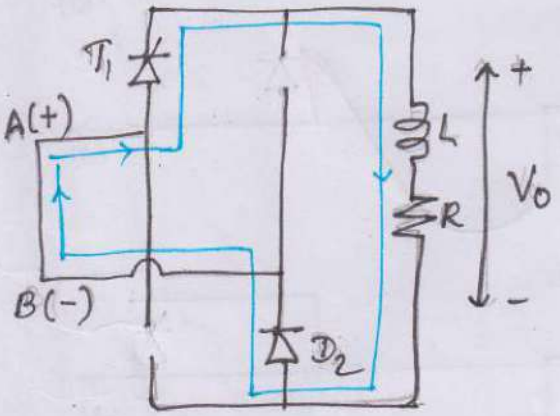


The conducting period of thyristors & diodes will be different.

L value large.

So load current continuous & so it is taken to be constant.

Mode 1: (α to π)

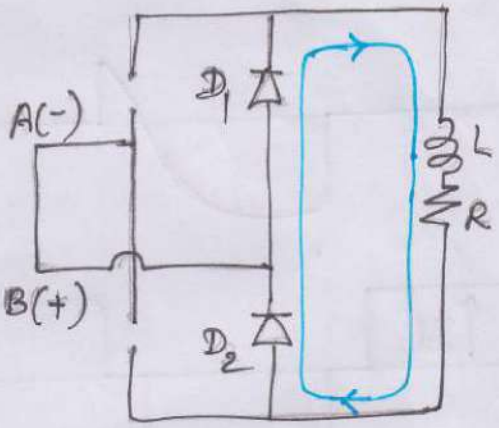


T_1 D_2 – FB

$A^{(+)} \rightarrow T_1 \rightarrow LR \rightarrow D_2 \rightarrow B^{(-)}$

V_o-(+)ve i_o-(+)ve

Mode 2: π to $\pi+\alpha$

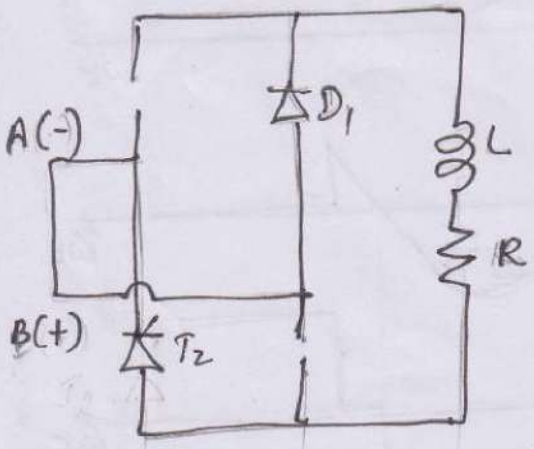


D_1 D_2 – FB

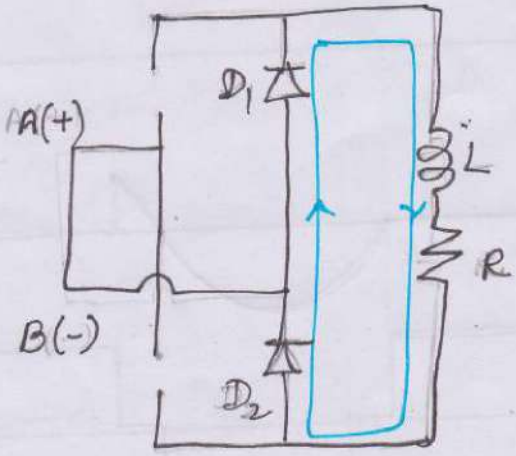
$LR \rightarrow D_2 \rightarrow D_1 \rightarrow LR$

V_o - +ve i_o - +ve

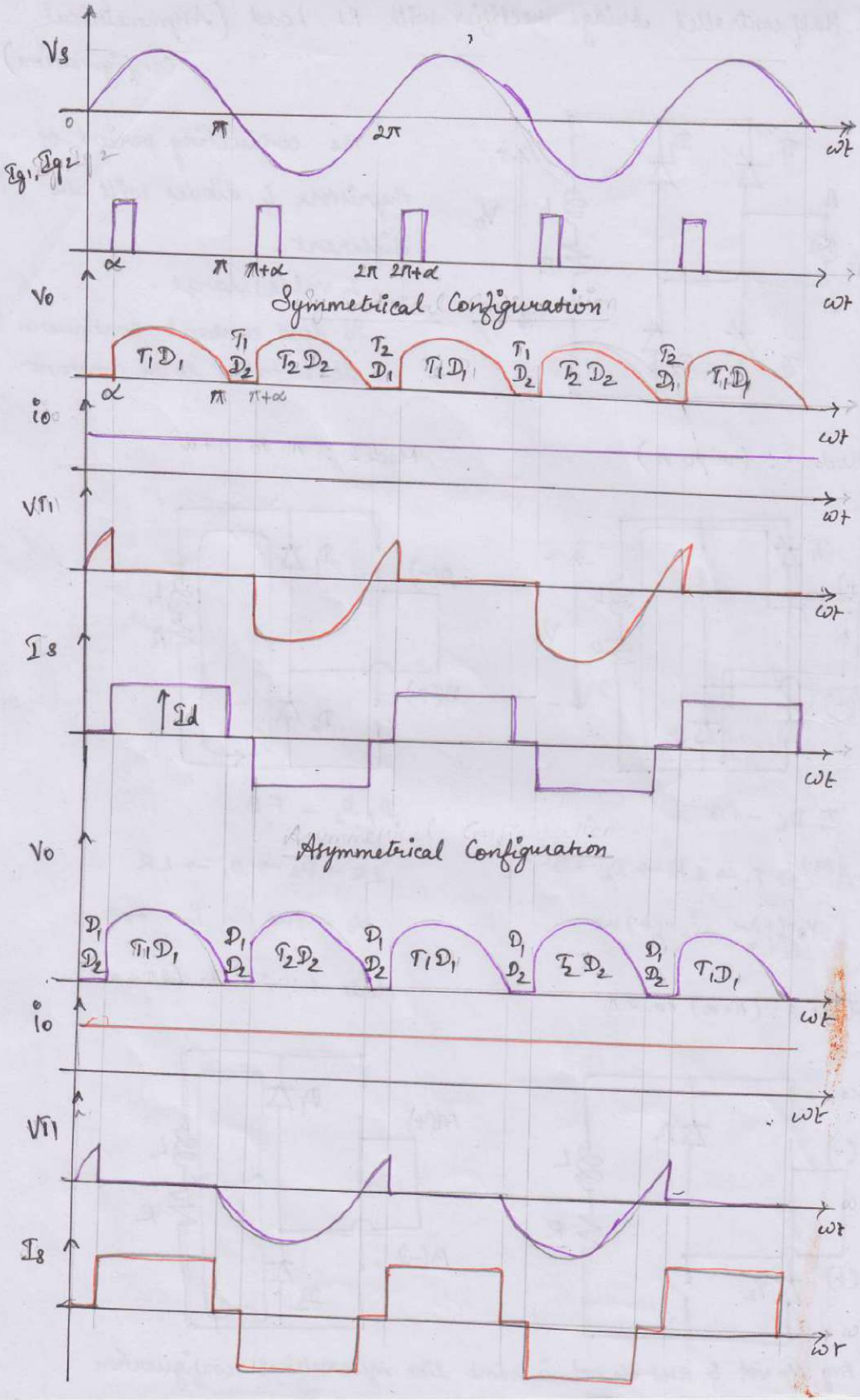
Mode 3: $(\pi+\alpha)$ to 2π



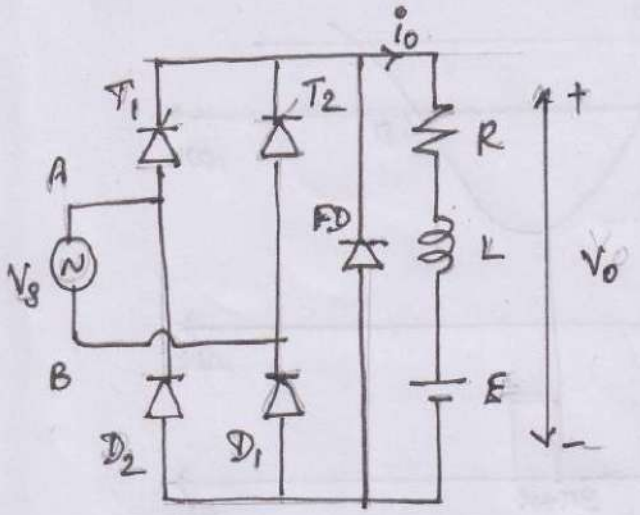
Mode 4: 2π to $(2\pi+\alpha)$



Avg o/p vol & RMS o/p vol is same like symmetrical configuration


Vs
0
π
2π
ωt
Tg1, Tg2
α
π
π+α
2π
2π+α
Vo
Symmetrical Configuration
T1 D1
T1 D2
T2 D2
T2 D1
T1 D1
T1 D2
T2 D2
T2 D1
T1 D1
α
π
π+α
io
ωt
VT1
ωt
Is
Id
ωt
Vo
Asymmetrical Configuration
D1 D2
T1 D1
D1 D2
T2 D2
D1 D2
T1 D1
D1 D2
T2 D2
D1 D2
T1 D1
io
ωt
VT1
ωt
Is
ωt

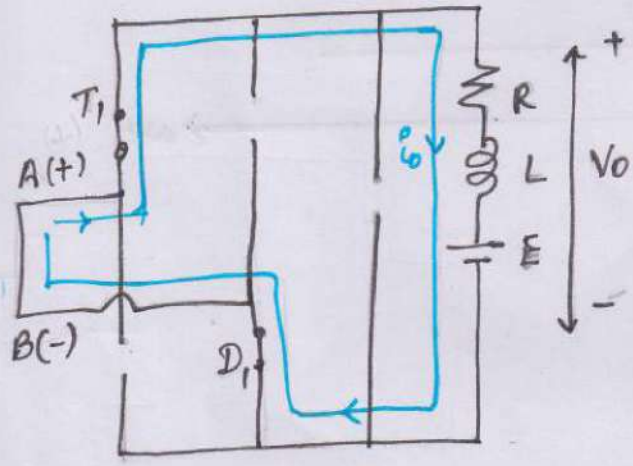
1φ Half controlled rectifier with RLE load and free wheeling Diode (Symmetrical Configuration)



Load inductance is assumed to be ~~continuous~~ large and load current is assumed continuous.

The thyristors will get forward biased only when source voltage V_s exceeds E. ie, $V_s > E$

mode 1 :- α to π



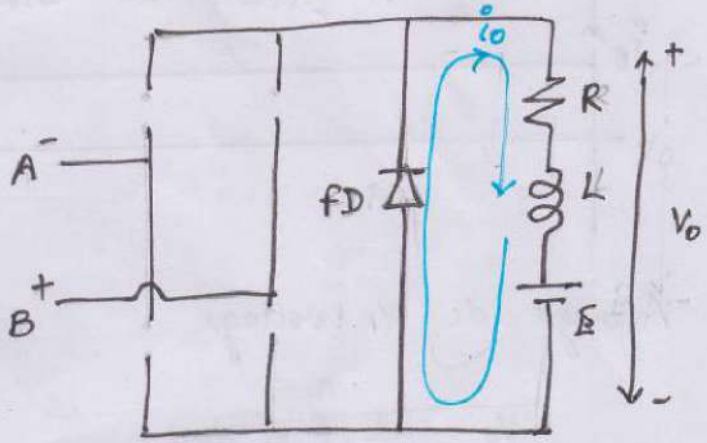
$T_1 D_1$ - FB.

$A^+ \rightarrow T_1 \rightarrow RLE \rightarrow D_1 \rightarrow B^-$

V_o = +ve

i_o = +ve

mode 2 : π to $\pi+\alpha$



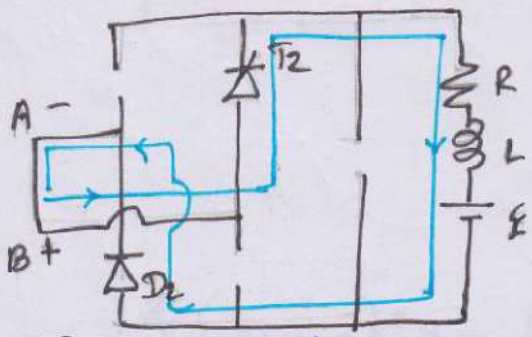
$T_1 D_1$ - off, FD - Forward biased

The freewheeling diode conducts to provide the continuity of current in the inductive load.

V_o = 0 i_o = +ve

$RLE \rightarrow FD \rightarrow RLE$

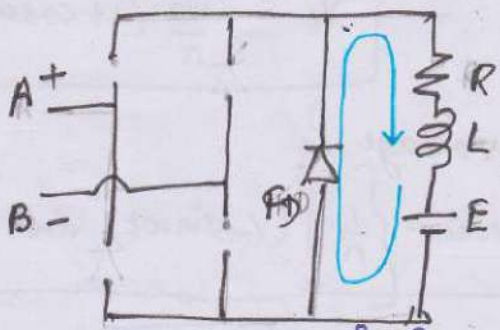
mode 3 : $\pi+\alpha$ to 2π



$T_2 D_2$ - FB $B^+ \rightarrow T_2 \rightarrow RLE \rightarrow D_2 \rightarrow A^-$

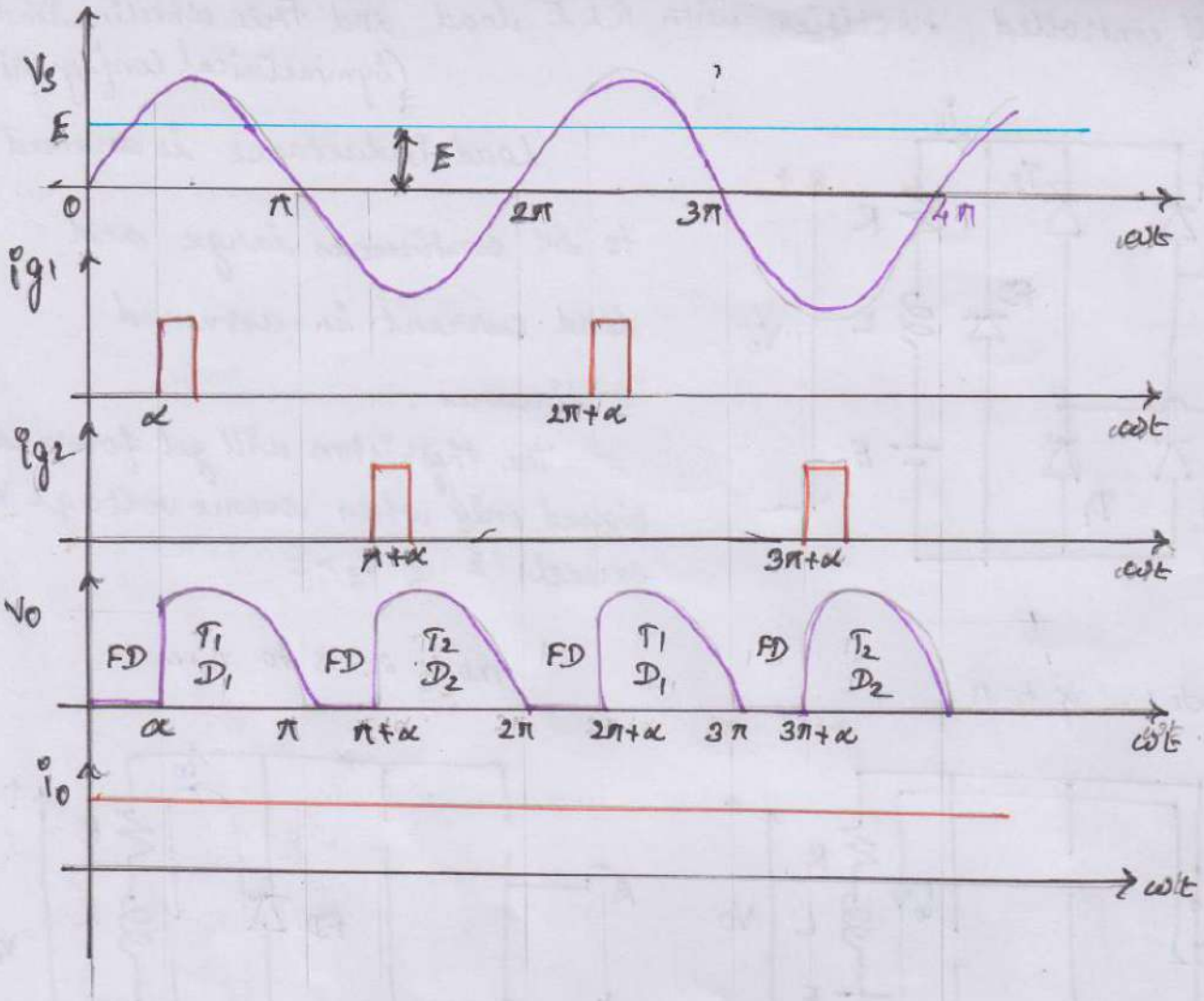
V_o = +ve i_o = +ve

mode 4 :- 2π to $2\pi+\alpha$



$T_2 D_2$ - off FD is FB

$RLE \rightarrow FD \rightarrow RLE$.



Average dc o/p voltage.

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\pi} V_s \, d\omega t$$

$$= \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi}$$

$$= -\frac{V_m}{\pi}\left[\cos\pi - \cos\alpha\right]$$

$$\boxed{V_o = \frac{V_m}{\pi}(1+\cos\alpha)}$$

RMS voltage.

$$V_{rms} = \left\{\frac{1}{\pi}\int_{\alpha}^{\pi}(V_m \sin\omega t)^2 \, d\omega t\right\}^{1/2}$$

$$\boxed{V_{rms} = \left\{\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi}\right\}^{1/2}} = \frac{V_m}{\sqrt{2\pi}}\left\{\pi - \alpha + \frac{\sin 2\alpha}{2}\right\}^{1/2}$$

3ϕ Controlled converters.

1ϕ supply → produces a relatively high proportion of a-c ripple-voltage at its d-c terminals which is an undesirable one.

Therefore, a smoothing reactor is necessary to smoothen the o/p voltage.

The need of smoothing can be minimised by increasing the number of pulses.

When the no of pulses of the converter is ↑ed, the no of segments that fabricate the o/p voltage also ↑s & consequently the ripple content ↓es.

3ϕ rectifier ckts are used for larger power applications.

Classification of 3ϕ controlled converters

1) 3-pulse converters
2) 6-pulse converters
3) 12-pulse converters.

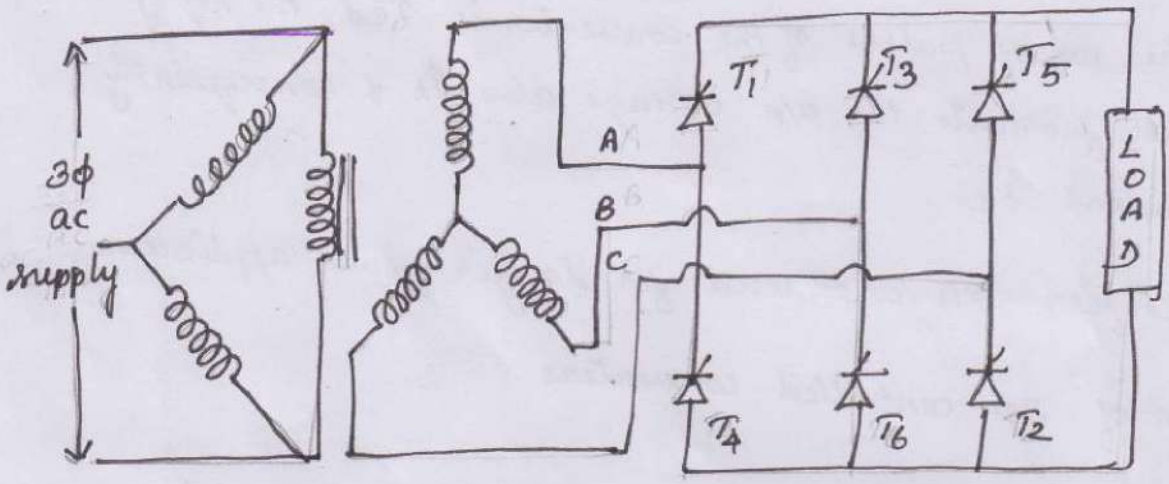
3-pulse converters are also known as 3ϕ half-wave controlled rectifier.

But the 3-pulse converters have not become very popular because of the fact that they require special types of converter transformer to prevent d-c magnetisation.

Six-pulse Converters have the following advantages compared to three-pulse converters

1) Commutation is made very easier.
2) Distortion on the a.c. side is reduced due to the reduction in lower-order harmonics.
3) Inductance required in series is considerably reduced

3ϕ Fully controlled bridge converter



The load is fed via a 3ϕ half-wave connection to one of the 3 supply lines, no neutral being required.

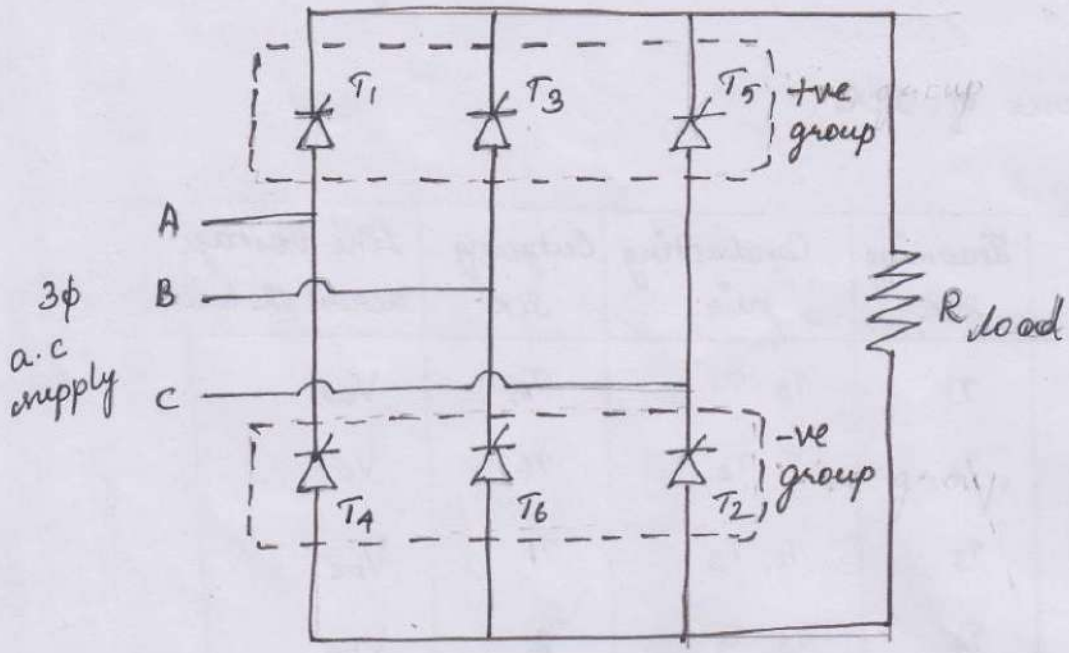
Hence transformer connection is optional.

However, for isolation of o/p from supply source, or for higher o/p requirements transformer is to be connected.

If it is used, one winding is connected in delta bcz the delta connection gives the circulating path for 3rd harmonic current.

∴ The 3rd order harmonic current does not appear in line which is an advantage.

3φ Fully controlled bridge rectifier with R-load.



* The ckt consists of 2 groups of SCRs, +ve group & -ve group.
* +ve group is formed by T_1, T_3 & T_5.
* -ve group is " " T_4, T_6 & T_2.
✓ The +ve group devices are turned-on when the supply voltages are +ve.
✓ The -ve group devices are turned-on when the supply voltages are -ve.
✓ To start the ckt functioning, 2 thyristors must be fired at the same time in order to commence current-flow, one of the upper arm and one of the lower arm.
* Each device should be triggered at a desired firing angle α
* Each SCR can conduct for 120°.
* SCRs must be triggered in the sequence T_1, T_2, T_3, T_4, T_5 & T_6
* The phase shift between the triggering of two adjacent SCRs is 60°.
* At any instant, two SCRs can conduct and there are such 6 pairs. (T_6 T_1), (T_1, T_2), (T_2 T_3), (T_3 T_4) (T_4 T_5) & (T_5 T_6)

* Each SCR conducts in 2 pairs & each pair conducts for 60°.

* The incoming SCR commutates the outgoing SCR.

Firing sequence of SCRs.

S. No	ωt	Incoming SCR	Conducting pair	Outgoing SCR	Line voltage across the load
1.	30° + α	T_1	T_6 T_1	T_5	V_{ab}
2	90° + α	T_2	T_1 T_2	T_6	V_{ac}
3	150 + α	T_3	T_2 T_3	T_1	V_{bc}
4	210 + α	T_4	T_3 T_4	T_2	V_{ba}
5	270 + α	T_5	T_4 T_5	T_3	V_{ca}
6	330 + α	T_6	T_5 T_6	T_4	V_{cb}.

* When two SCRs are conducting, ie, one from +ve group & one from -ve group, the corresponding line voltage is applied across the load.

For 6-pulse operation, each SCR has to be fired twice in its conduction cycle, that is firing intervals should be 60°.

The o/p voltage waveform for any value of α is a 6 pulse wave with a ripple frequency of 300 Hz.

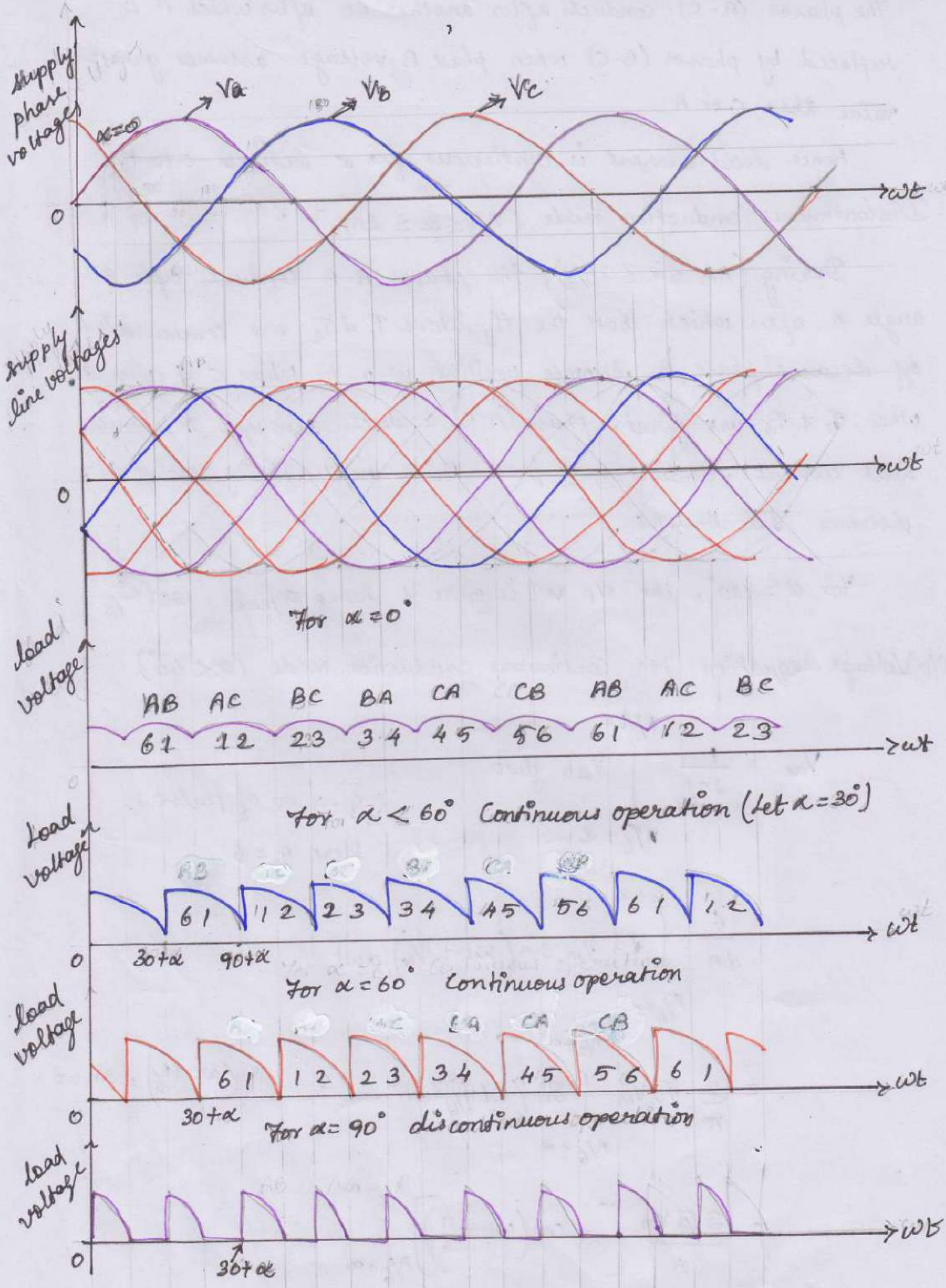
Continuous conduction mode ($0 \le \alpha \le \pi/3$ or $60°$)

$\alpha = 30°$

When the phasor (A-B) is allowed to conduct at α between 0 to π/3, it continues to conduct by 60° when the phasor (A-C) is fired.

The conduction is shifted from SCR T_6 to T_2.

T_6 is commutated by the reverse-voltage of phase C & B across it.


Supply phase voltages
Va
Vb
Vc
α=0
0
ωt
Supply line voltages
0
ωt
For α=0°
Load voltage
AB AC BC BA CA CB AB AC BC
61 12 23 34 45 56 61 12 23
ωt
For α<60° Continuous operation (let α=30°)
Load voltage
61 12 23 34 45 56 61 12
ωt
0
30+α
90+α
For α=60° Continuous operation
Load voltage
61 12 23 34 45 56 61
ωt
0
30+α
For α=90° discontinuous operation
Load voltage
ωt
0
30+α

The phasor (A-C) conducts after another 60° after which it is replaced by phasor (B-C) when phase B voltage assumes greater value than C or A.

Hence load current is continuous for α between 0 to $\pi/3$.

Discontinuous conduction mode ($\pi/3 \le \alpha \le 2\pi/3$)

During ($\pi/3 \le \alpha \le 2\pi/3$), the phasor A-B conducts upto an angle π after which both the thyristors T_1 & T_6 are commutated off because phase B becomes positive w.r. to phase C & after 60°. when T_2 & T_1 are fired, phase (A-C) conducts also upto π, hence load current remains zero from π to next firing pulse & becomes discontinuous.

for $\alpha = 120°$, the o/p vol is zero & hence $\alpha_{max} = 120° (2\pi/3)$

O/p Voltage equation for continuous conduction mode ($\alpha < 60°$)

$$V_{dc} = \frac{1}{2\pi/q} \int_{\pi/6+\alpha}^{\pi/2+\alpha} V_{ab}\, d\omega t$$

$q \rightarrow$ no of pulses.

Here $q = 6$

$$= \frac{6}{2\pi} \int_{\pi/6+\alpha}^{\pi/2+\alpha} \sqrt{3}\, V_m \sin\left(\omega t + \pi/6\right) d\omega t.$$

$$= \frac{3}{\pi} \sqrt{3}\, V_m \int_{\pi/6+\alpha}^{\pi/2+\alpha} \sin\left(\omega t + \pi/6\right) d\omega t$$

$\sin\left(\omega t + \pi/6\right) = \sin\omega t$.

$$= \frac{3\sqrt{3}\, V_m}{\pi} \left[-\cos\left(\omega t + \frac{\pi}{6}\right) \right]_{\pi/6+\alpha}^{\pi/2+\alpha}$$

$$= -\frac{3\sqrt{3}\, V_m}{\pi} \left[\cos\left(\frac{\pi}{2} + \alpha + \frac{\pi}{6}\right) - \cos\left(\frac{\pi}{6} + \alpha + \pi/6\right) \right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[\cos\left(\frac{2\pi}{3}+\alpha\right) - \cos\left(\frac{\pi}{3}+\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[\left(\cos\frac{2\pi}{3}\cos\alpha - \sin\frac{2\pi}{3}\sin\alpha\right) - \left(\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[\left(-\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right) - \left(\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[-\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha - \frac{1}{2}\cos\alpha + \frac{\sqrt{3}}{2}\sin\alpha\right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left(-\frac{2\cos\alpha}{2}\right)$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}V_m}{\pi}\cos\alpha}$$ ✓ for R & RL

Average load current (I_{dc})

$$\boxed{I_{dc} = \frac{V_{dc}}{R} = \frac{3\sqrt{3}V_m}{\pi R}\cos\alpha}$$

O/p voltage equation for discontinuous conduction mode ($\alpha > 60^\circ$)

$$V_{dc} = \frac{6}{2\pi}\int_{\pi/6+\alpha}^{5\pi/6} \sqrt{3}V_m \sin\left(\omega t + \frac{\pi}{6}\right) d\omega t$$

$$= \frac{3\sqrt{3}V_m}{\pi}\int_{\pi/6+\alpha}^{5\pi/6} \sin\left(\omega t + \pi/6\right) d\omega t$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-\cos\left(\omega t + \frac{\pi}{6}\right)\right]_{\pi/6+\alpha}^{5\pi/6}$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[\cos\left(\frac{5\pi}{6}+\frac{\pi}{6}\right) - \cos\left(\frac{\pi}{6}+\alpha+\frac{\pi}{6}\right)\right]$$

$$= -\frac{3\sqrt{3}V_m}{\pi}\left[\cos\frac{2\pi}{6} - \cos\left(\frac{2\pi}{6_3}+\alpha\right)\right]$$

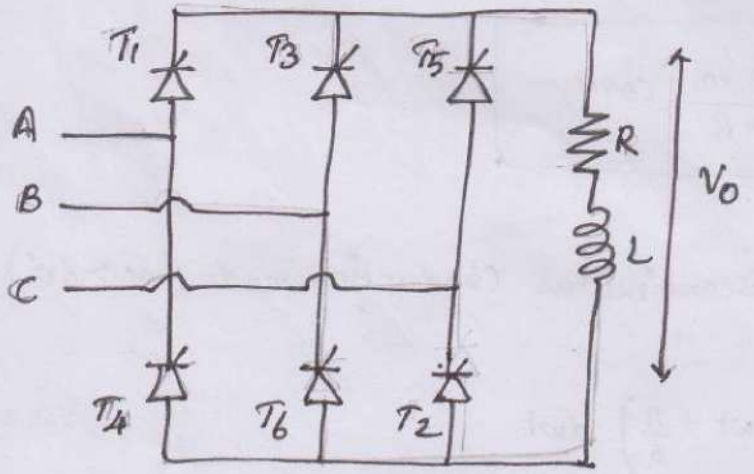
$$= -\frac{3\sqrt{3}V_m}{\pi}\left[-1 - \cos\left(\frac{\pi}{3}+\alpha\right)\right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}V_m}{\pi}\left[1 + \cos\left(\frac{\pi}{3}+\alpha\right)\right]}$$

Avg load current

$$\boxed{I_{dc} = \frac{V_{dc}}{R} = \frac{3\sqrt{3}}{\pi R}\left[1 + \cos\left(\frac{\pi}{3}+\alpha\right)\right]}$$

3ϕ fully controlled bridge rectifies with RL Load



The load inductance is assumed to be very large so as to produce a constant load current.

Operation & Conduction sequence same like R load.

Waveforms are similar with R-load for $\alpha = 0^\circ, 30^\circ + 60^\circ$

✓ For $\alpha > 60^\circ$, the waveforms are different.

✓ Because of inductive nature of load, the voltage goes -ve.

✓ The previous thyristor pair continuous to conduct till the next SCR is triggered.

For eg: T_5 & T_1 continuous to conduct upto $(90+\alpha)$ till thyristor T_2 is triggered and when T_2 is triggered it commutates the SCR T_6 and so T_1 & T_2 starts conducting.

✓ For $\alpha = 90^\circ$, the area under the +ve & -ve cycle are equal & the average voltage is zero.

✓ For $\alpha < 90^\circ$, the average o/p voltage is positive

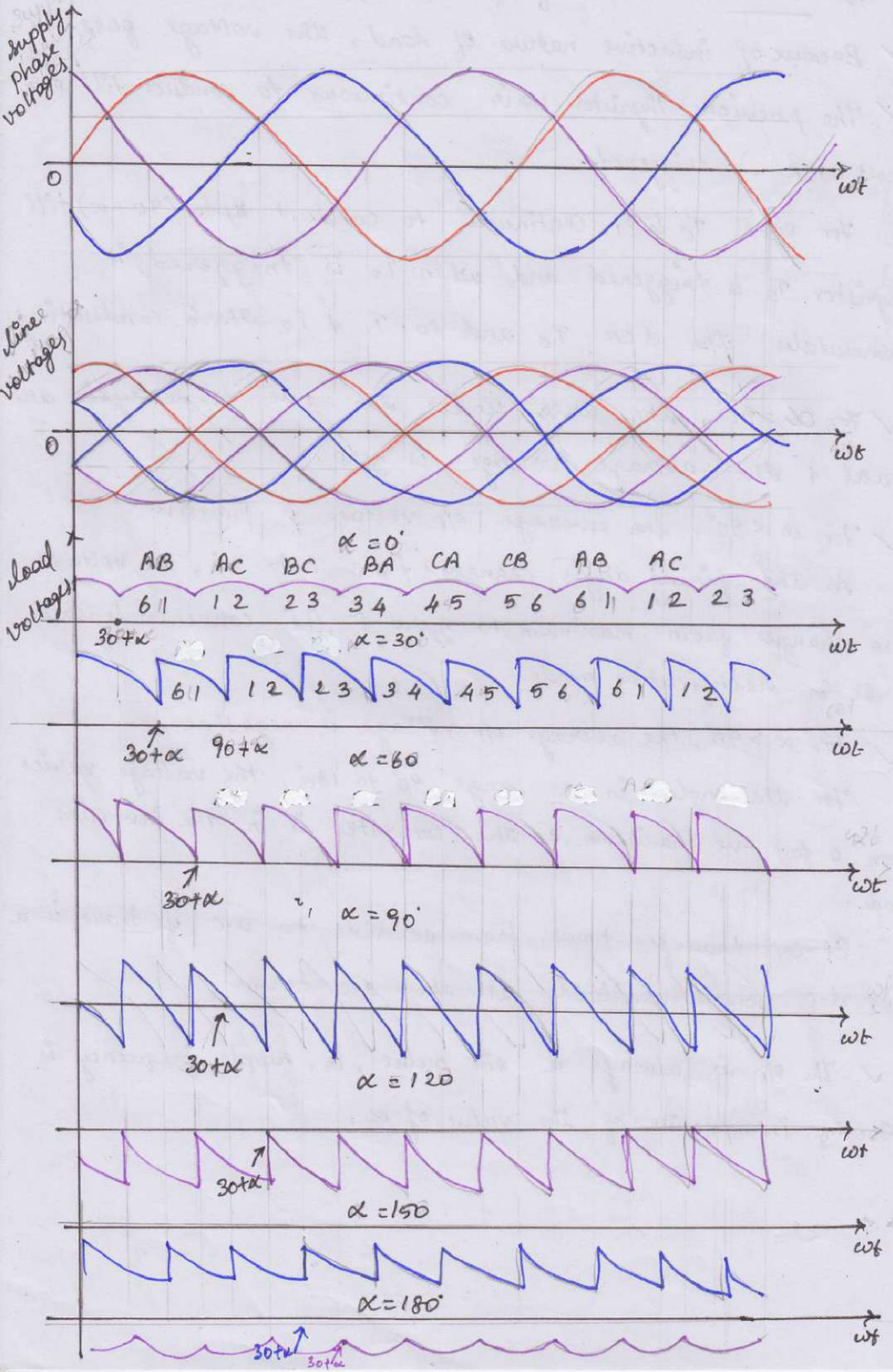
As the firing angle changes from 0 to 90°, the voltage also changes from maximum to zero & the converter is said to be in rectification mode.

✓ For $\alpha > 90^\circ$, the average o/p voltage is negative.

For the angles in the range 90° to 180°, the voltage varies from 0 to -ve maximum & the converter is in the inversion mode.

~~It can transfer power from dc side to a.c if there is a -ve d.c source available at the d.c term~~

✓ The o/p is always a six pulse, ie, ripple frequency is 300Hz irrespective of the value of α.


supply phase voltages
0
ωt
line voltages
0
ωt
load voltages
α = 0°
AB AC BC BA CA CB AB AC
6 1 1 2 2 3 3 4 4 5 5 6 6 1 1 2 2 3
ωt
30+α
α = 30°
6 1 1 2 2 3 3 4 4 5 5 6 6 1 1 2
ωt
30+α
90+α
α = 60
ωt
30+α
α = 90°
ωt
30+α
α = 120
ωt
30+α
α = 150
ωt
α = 180°
ωt
30+α
30+α

Average o/p voltage and current similar to R load of continuous conduction

$$V_{dc} = \frac{3\sqrt{3}\,V_m}{\pi}\cos\alpha \quad \text{for } (0 \le \alpha \le 180^\circ)$$

$\alpha < 90$ → rectification mode.

$\alpha > 90$ → inversion mode.

RMS o/p voltage.

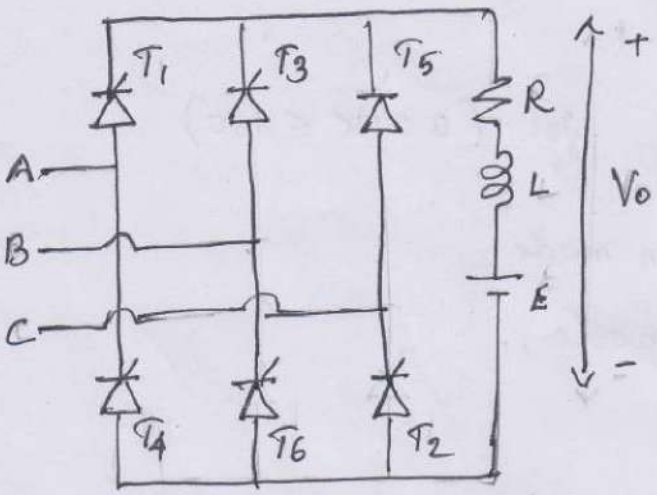
$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} V_{dc}^2(\omega t)\, d\omega t\right]^{1/2}$$

$$= \left\{\frac{6}{2\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha} \left[V_{ab}(\omega t)\right]^2 d\omega t\right\}^{1/2}$$

$$= \left\{\frac{9V_m^2}{2\pi}\left[60^\circ + \frac{1}{2}\left(\sqrt{3}\cos 2\alpha\right)\right]\right\}^{1/2}$$

$$= \left[\frac{3V_m}{2}\left(\frac{2}{3} + \frac{\sqrt{3}}{\pi}\cos 2\alpha\right)\right]^{1/2}$$

3φ Full bridge converters with RLE Load



The 3φ full bridge converter will works as a 3φ ac to dc converter for firing angle delay $0° < \alpha \leq 90°$ and as 3φ line-commutated inverter for $90° < \alpha < 180°$.

Thus this 3φ full converter is preferred where regeneration of power is required.

For $\alpha = 0°$, T_1 to T_6 behave like diodes.

For $\alpha = 60°$, T_1 is triggered at $\omega t = 30° + 60 = 90°$.

Similarly T_2 triggered at $\omega t = 90 + 60 = 150$ & so on.

Each SCR conducts for 120°.

Conduction sequence : $T_5\ T_6$

$T_6\ T_1$

$T_1\ T_2$

$T_2\ T_3$

$T_3\ T_4$

$T_4\ T_5$

$T_5\ T_6$ .. & repeats

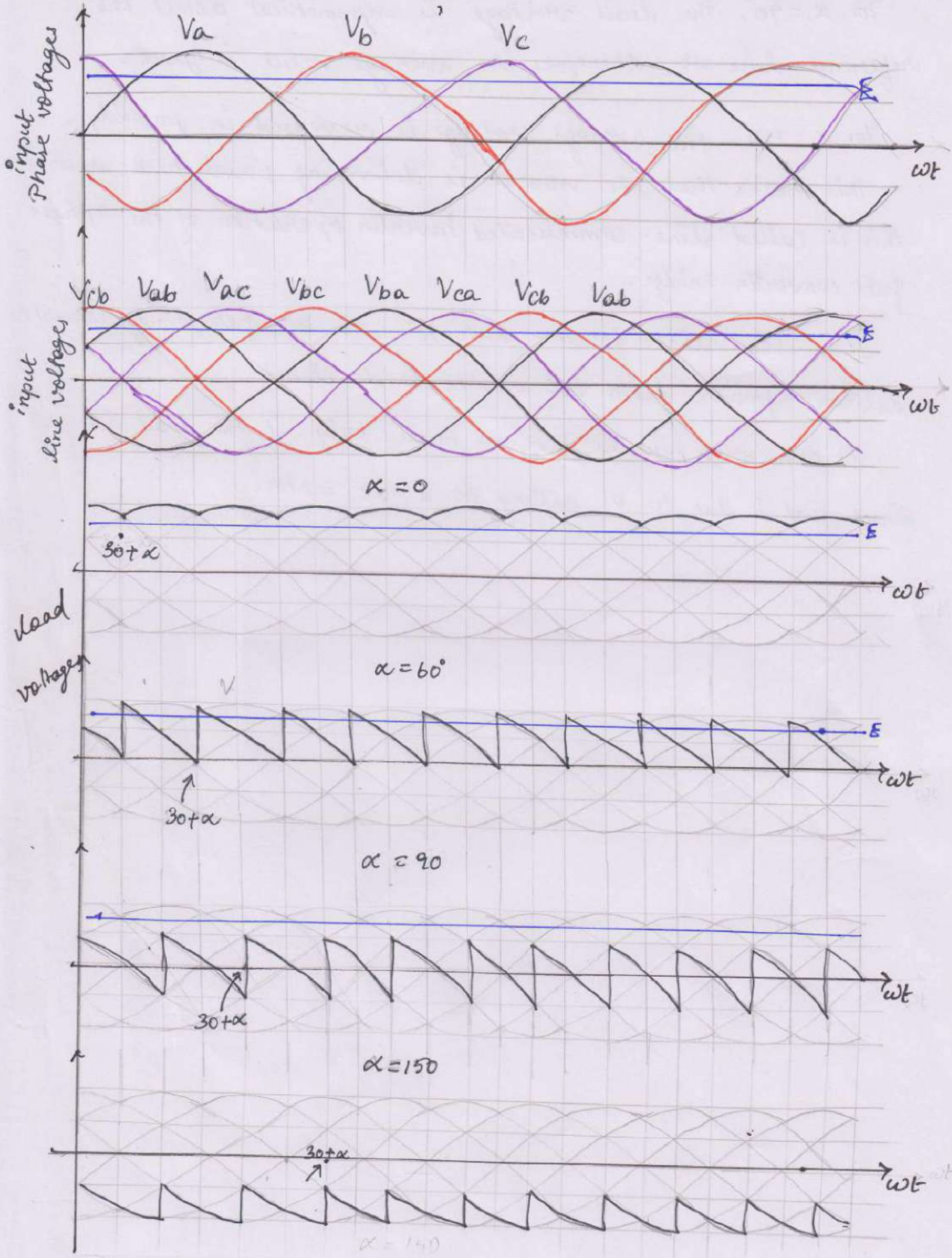
The SCRs from both the groups (positive or negative) are fired at an interval of 60°.

This means that commutation occurs every 60°

When T_1 is turned on, T_5 is turned off. T_6 is already Conducting.

As T_1 & T_6 are connected to A & B, load voltage must be V_{ab}.

When T_2 is turned on, T_6 is commutated.


Va
Vb
Vc
input Phase voltages
ωt
Vcb Vab Vac Vbc Vba Vca Vcb Vab
input line voltages
E
α = 0
30+α
Load voltage
α = 60°
α = 90
α = 150

For $\alpha = 90^\circ$, the load voltage is symmetrical about the reference line ωt, therefore its average value is zero.

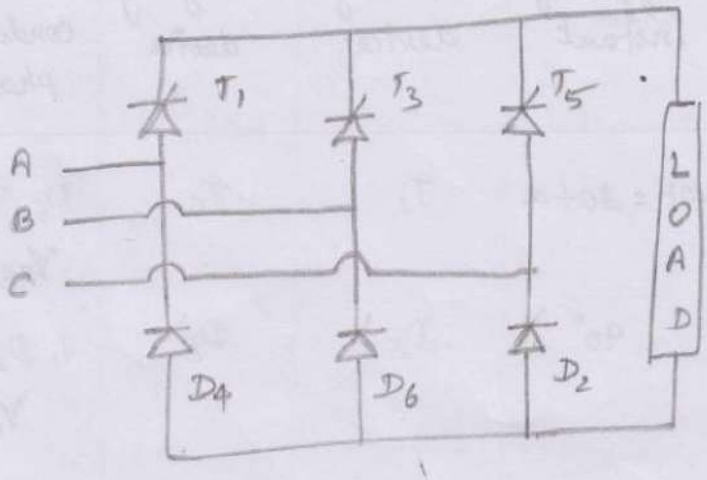
For $\alpha = 150^\circ$, the average voltage is reversed in polarity. This means that dc source is delivering power to ac source; this is called line-commutated inverter operation of the 3phase full converter bridge.

It is seen that for $\alpha = 0^\circ$ to 90°, the 3ϕ full bridge converter delivers power from ac source to dc load.

It can work in the inverter mode only if the load has a direct emf E due to a battery or a dc motor.

3ϕ Half controlled bridge converter / (3ϕ semi converter) (or) 3-pulse converter.

The circuit contains 3 SCRs & 3 diodes.

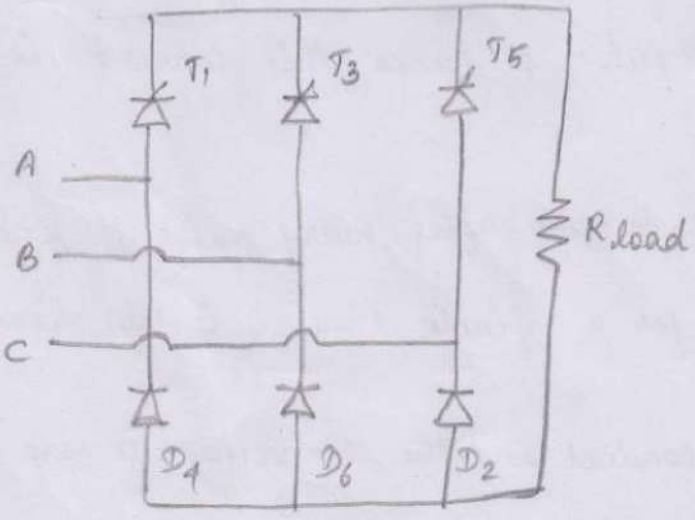


Here asymmetrical configuration is not used because it introduces imbalance in line-currents on the a.c side.

Operates in one quadrant only. Hence can be used for industrial applications upto 120 kW level.

If delay angle of this converter is 1ed, the P.F is 1ed.

Operation with Resistive load.



*) Diode starts conducting as soon as they are forward-biased

* Line voltages conducts in the sequence V_{AB}, V_{AC}, V_{BC}, V_{BA}, V_{CA} and V_{CB}.

* A line voltage which has the highest value compared to others will conduct, ie, when it makes an angle of 60° with neutral.

Incoming, Outgoing & conducting devices.

S. No	Triggering instant	Incoming device	Outgoing device	Pair conducting & phasor	Conducting period of each pair	conducting period of outgoing device
1.	$\omega t = 30 + \alpha$	T_1	T_5	$D_6\ T_1$ V_{AB}	$60 - \alpha$	120°
2.	90°	D_2	D_6	$T_1\ D_2$ V_{AC}	$60 + \alpha$	120°
3.	$150 + \alpha$	T_3	T_1	$D_2\ T_3$ V_{BC}	$60 - \alpha$	120°
4.	210	D_4	D_2	$T_3\ D_4$ V_{BA}	$60 + \alpha$	120°
5.	$270 + \alpha$	T_5	T_3	$D_4\ T_5$ V_{CA}	$60 - \alpha$	120°
6	330	D_6	D_4	$T_5\ D_6$ V_{CB}	$60 + \alpha$	120°

✓ For $\alpha = 0^\circ$, the o/p voltage waveform is a 6 pulse o/p.

✓ For $\alpha \geq 30^\circ$, the o/p is only a 3 pulse & hence this converter is known as 3-pulse converter.

✓ The o/p voltage waveforms goes to zero after every pulse for $\alpha = 60^\circ$ & for $\alpha > 60^\circ$, it remains zero for a finite time & is thus discontinuous

✓ For $\alpha = 180^\circ$, no phasor can conduct and the o/p voltage is zero

For $\alpha \le 60°$, Average dc o/p voltage

$$V_{dc} = 3 \times \frac{1}{2\pi}\left[\int_{30+\alpha}^{90} V_{ab}\, d\omega t + \int_{90}^{150+\alpha} V_{ac}\, d\omega t\right]$$

$$= \frac{3}{2\pi}\left[\int_{30+\alpha}^{90} \sqrt{3}\, V_m \sin(\omega t + 30)\, d\omega t + \int_{90}^{150+\alpha} \sqrt{3}\, V_m \sin(\omega t - 30)\, d\omega t\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[\int_{30+\alpha}^{90} \sin(\omega t + 30)\, d\omega t + \int_{90}^{150+\alpha} \sin(\omega t - 30)\, d\omega t\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left\{\left[-\cos(\omega t + 30)\right]_{30+\alpha}^{90} + \left[-\cos(\omega t - 30)\right]_{90}^{150+\alpha}\right\}$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[-\left[\cos(90+30) - \cos(60+\alpha)\right] - \left[\cos(120+\alpha) - \cos 60\right]\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[-(-\sin 30) + \cos(60+\alpha) - \cos(120+\alpha) + \cos 60\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[+\frac{1}{2} + \cos(60+\alpha) - \cos(120+\alpha) + \frac{1}{2}\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[1 + \cos(60+\alpha) - \cos(120+\alpha)\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[1 + (\cos 60 \cos\alpha - \sin 60 \sin\alpha) - (\cos 120 \cos\alpha - \sin 60 \sin\alpha)\right]$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[1 + \frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha + \frac{1}{2}\cos\alpha + \frac{\sqrt{3}}{2}\sin\alpha\right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}\, V_m}{2\pi}(1 + \cos\alpha)}$$

For $\alpha \geq 60^\circ$,

$$V_{dc} = \frac{3}{2\pi}\left[\int_{30+\alpha}^{210} V_{ac}\, d\omega t\right]$$

$$= \frac{3}{2\pi}\int_{30+\alpha}^{210} \sqrt{3}\, V_m \sin(\omega t - 30)\, d\omega t$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[-\cos(\omega t - 30)\right]_{30+\alpha}^{210}$$

$$= -\frac{3\sqrt{3}\, V_m}{2\pi}\left[\cos 180 - \cos(30 + \alpha - 30)\right]$$

$$= \frac{-3\sqrt{3}\, V_m}{2\pi}\left[-1 - \cos\alpha\right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}\, V_m}{2\pi}(1 + \cos\alpha)}$$

RMS o/p voltage

$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} V_{dc}^2\, d\omega t\right]^{1/2}.$$

For $\alpha \leq 60^\circ$

$$= \left\{\frac{3}{2\pi}\left[\int_{30+\alpha}^{90} V_{ab}^2(\omega t)\, d\omega t + \int_{90}^{150+\alpha} V_{ac}^2(\omega t)\, d\omega t\right]\right\}^{1/2}$$

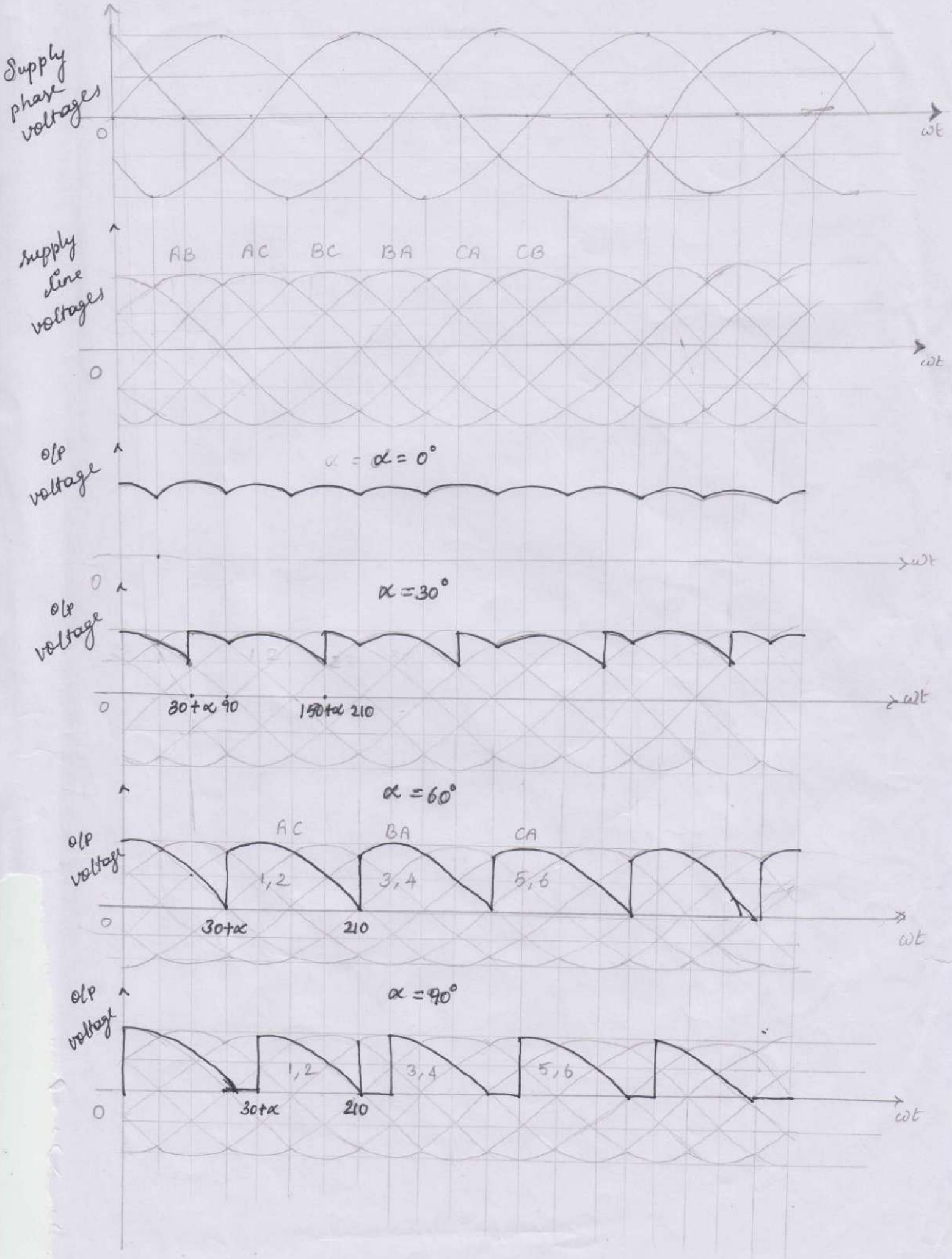
$$\boxed{V_{rms} = \frac{3}{2} V_m \left[\frac{2}{3} + \frac{\sqrt{3}}{2\pi}(1 + \cos 2\alpha)\right]^{1/2}}$$

For $\alpha > 60^\circ$

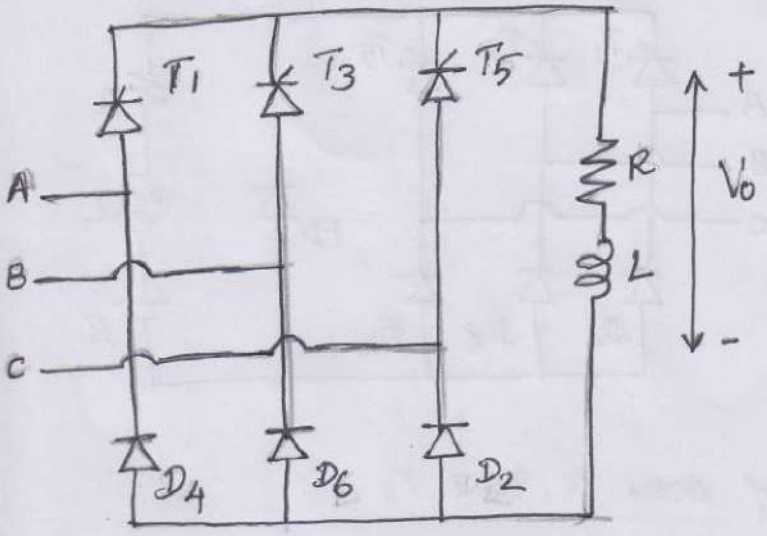
$$V_{rms} = \left\{\frac{3}{2\pi}\int_{30+\alpha}^{210} V_{ac}^2(\omega t)\, d\omega t\right\}^{1/2}$$

$$\boxed{V_{rms} = \frac{3\, V_m}{2}\left[\frac{\pi - \alpha + \frac{1}{2}\sin 2\alpha}{\pi}\right]^{1/2}}$$

3ϕ Half controlled bridge rectifier (R load) & RL Load.



3ϕ Half controlled converter with RL Load.



The value of inductance (L) is assumed to be so large.

Hence the o/p current is continuous waveform.

The voltage waveform is ||lr to that of Resistive load.

Hence, the avg & RMS values of o/p voltage waveform are same.

Continuous conduction mode.

The o/p voltage waveform is continuous for $\alpha < 60^\circ$ & is ripple free as shown for $\alpha = 30^\circ$.

The Form factor of current waveform is unity & the ripple factor is zero.

Discontinuous conduction mode.

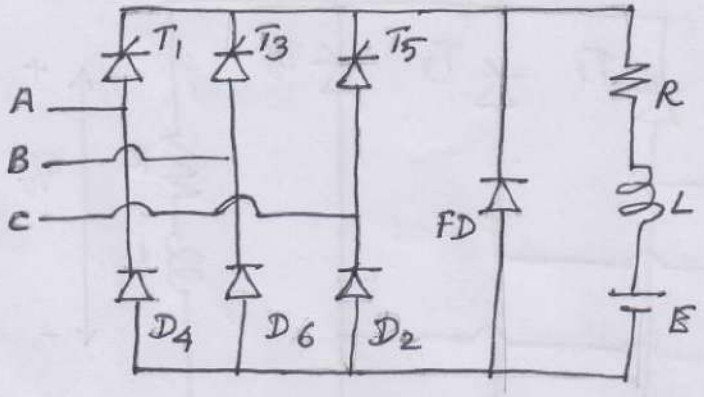
For $\alpha > 60^\circ$, the o/p voltage becomes zero during a part of the o/p voltage period because of freewheeling action.

Waveforms & avg o/p voltages are ||lr to 3ϕ semiconverter with R load.

$$\text{i.e., } V_{o(avg)} = \frac{3\sqrt{3}\,V_m}{2\pi}(1+\cos\alpha)$$

3φ Semiconverter with RLE load & FD

A free wheeling diode FD, is connected in parallel with RLE load, ie, across the o/p terminals of the semiconverter.



The o/p voltage V_o across the load terminals is controlled by varying the firing angles of SCRs T_1, T_3 & T_5.

The diodes D_4, D_6 & D_2 provide merely a return path for the current to the most negative line terminal.

Each SCR & diode conduct for 120°.

For $\alpha = 0°$, the thyristors T_1, T_3 & T_5 would behave as diodes & the o/p voltage of semiconverter would be symmetrical 6-pulse per cycle.

A 3φ semiconverter has the unique feature of working as a 6-pulse converter for $\alpha < 60°$ and as a 3pulse converter for $\alpha \geq 60°$.

For $\alpha = 60°$, the thyristors are fired so that current returns through one diode during each 120° conduction period.

For voltage V_{ac}, T_1 and D_2 conduct simultaneously for 120°.

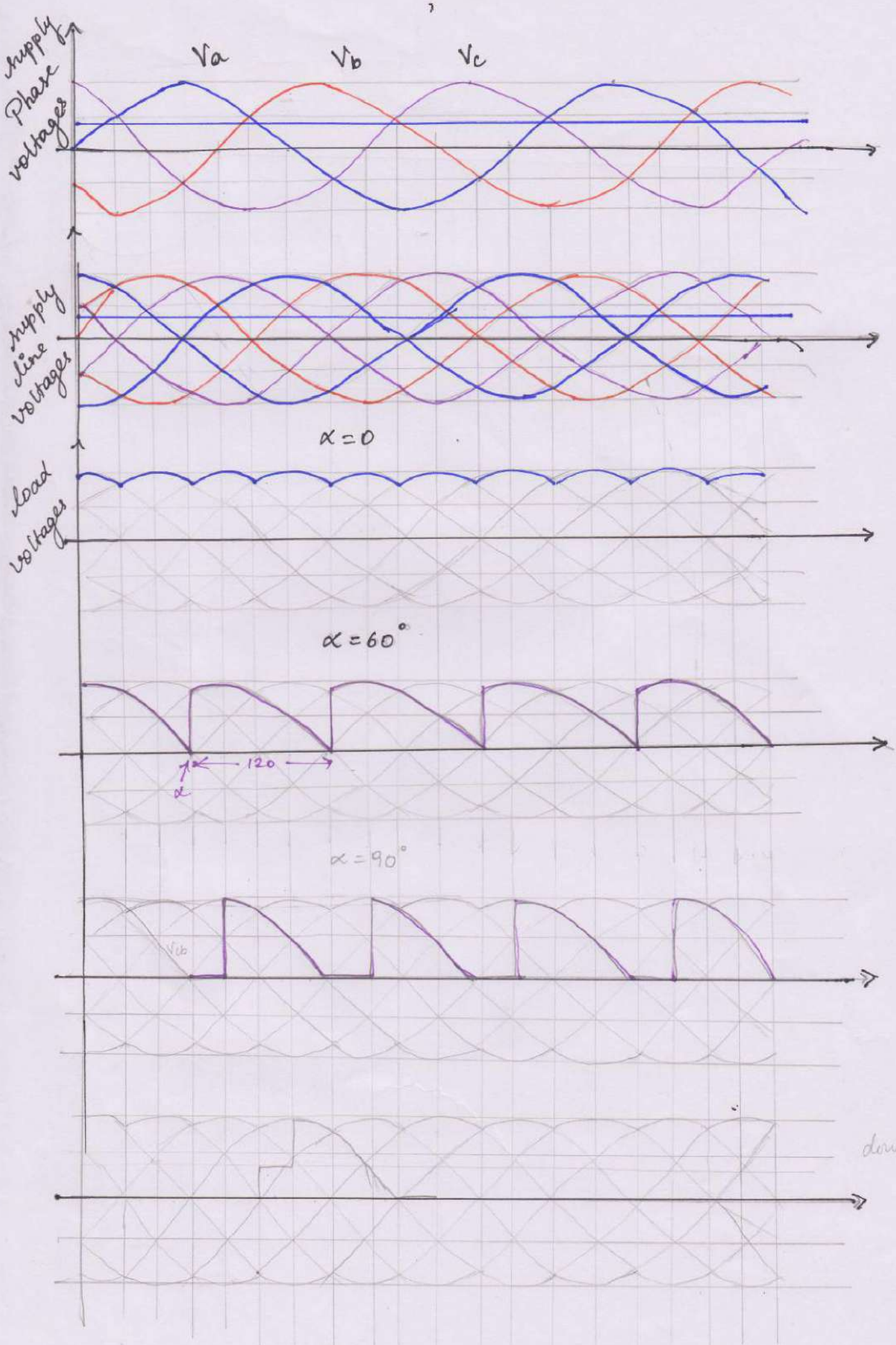
Similarly other elements conduct.

The freewheeling diode doesnot come into play even for $\alpha = 60°$.

The voltage pulses V_{ab}, V_{bc}, V_{ca} donot appear in the o/p voltage waveform for $\alpha \geq 60°$.

For firing angle delay of 90°, the o/p voltage V_o is discontinuous.

For $\alpha = 90°$, the conduction angle of SCRs and diodes is seen to be less than 120° for enery o/p pulse.


supply Phase voltages
Va
Vb
Vc
supply line voltages
α = 0
load voltages
α = 60°
120
α
α = 90°
doubt.

Dual converters

✓ Semiconverters are single quadrant converters

✓ The avg the voltage and current of the semiconverter indicates rectification mode & the power flow from ac source to dc load.

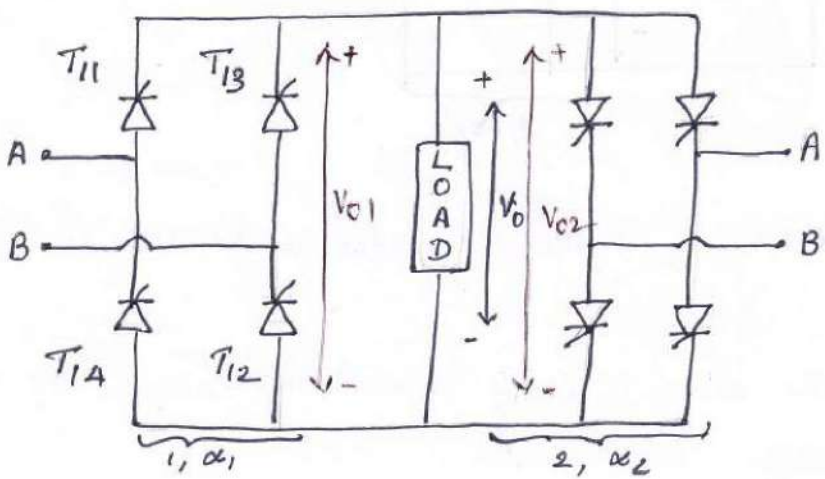
✓ The full converters operates as a rectifier in first quadrant (both V_o I_o - +ve) from $\alpha = 0°$ to $90°$ & as an inverter (V_o - -ve but I_o - +ve) from $\alpha = 90°$ to $180°$ in the fourth quadrant. Thus, the full converters are two quadrant converters.

✓ Incase four quadrant operation is required without any mechanical changeover switch, two full converters can be connected back to back to the load ckt. Such an arrangement using two full converters in antiparallel & connected to the same dc load is called a dual converter.

✓ There are 2 functional modes of a dual converter. one is non-circulating current mode & the other is circulating current mode.

Dual converter without circulating current

* With non-circulating current dual converter, only one converter is in operation at a time and it alone carries the entire load current.
* Only this converter receives the firing pulses from the trigger control.
* The other converter is blocked from conduction; this is achieved by removing the firing pulses from this converter.
* Such an arrangement for the dual converters has no reactor in-between the two converters.



* Suppose converter 1 is in operation & is supplying the load current.

* For blocking converter 1 and switching on converter 2, first the firing pulses to converter 1 are immediately removed or the firing angle of converter 1 is increased to maximum value & then its firing pulses are blocked.

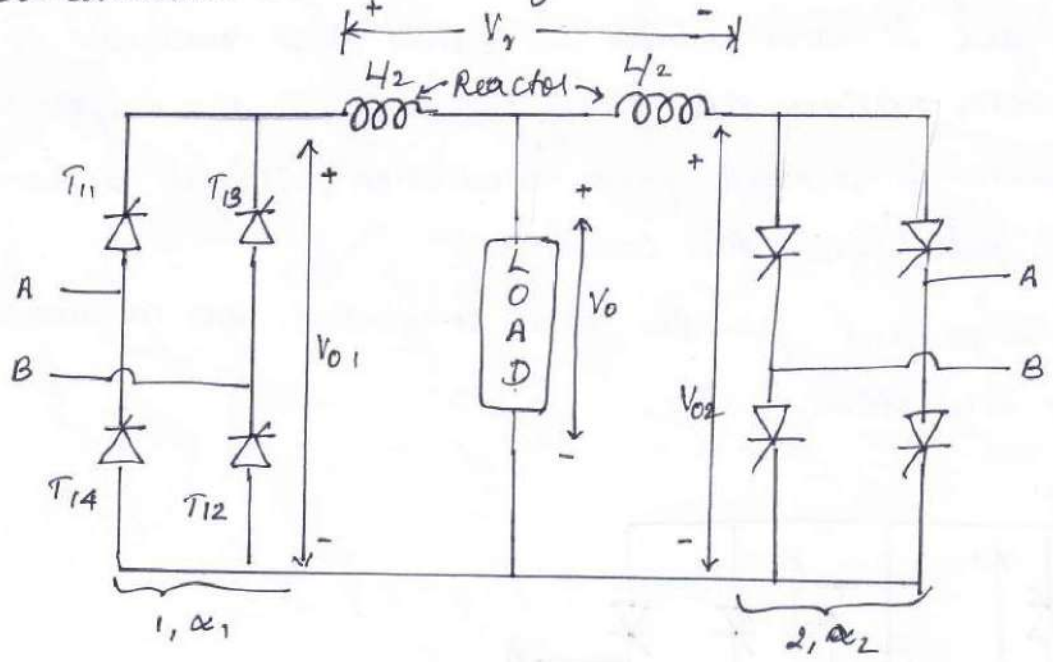
* With this, load current would decay to zero & then only converter 2 is made to conduct by applying the firing pulses to it.

* It should be ensured that during changeover from one converter to the other, the load current must decay to zero.

* After the outgoing converter has stopped conducting, a delay time of 10 to 20 msec is introduced before the firing pulses are applied to switch on the incoming converter.

* If the incoming converter is triggered before the outgoing converter has been completely turned-off a large circulating current would flow between the two converters.

Dual converter with circulating current.



• In the circulating mode of dual converter, a reactor is inserted in-between converters 1 & 2.

• This reactor limits the magnitude of circulating current to a reasonable value.

Dual converters

✓ Semiconverters are single quadrant converters

✓ The avg the voltage and current of the semiconverter indicates rectification mode & the power flow from ac source to dc load.

✓ The full converters operates as a rectifier in first quadrant (both V_o I_o - +ve) from $\alpha = 0°$ to $90°$ & as an inverter (V_o - -ve but I_o - +ve) from $\alpha = 90°$ to $180°$ in the fourth quadrant. Thus, the full converters are two quadrant converters.

✓ Incase four quadrant operation is required without any mechanical changeover switch, two full converters can be connected back to back to the load ckt. Such an arrangement using two full converters in antiparallel & connected to the same dc load is called a dual converter.

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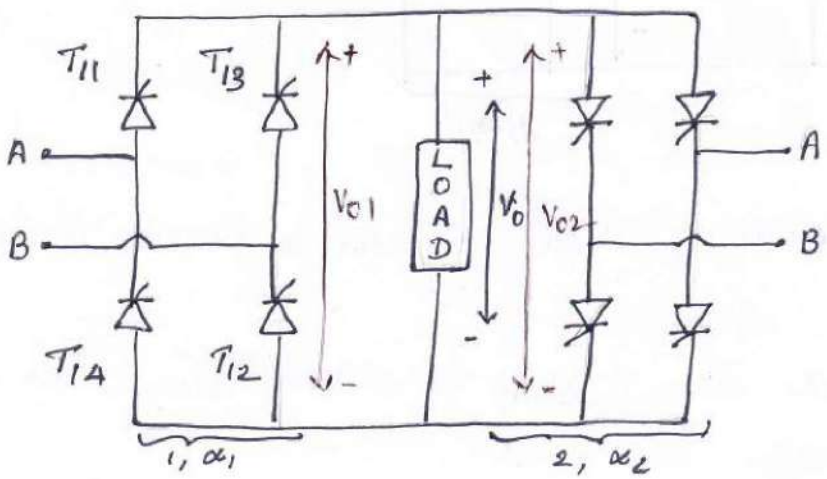


The firing pulses of the two converters are so adjusted that $\alpha_1 + \alpha_2 = 180°$.

For eg, if firing angle of conv-1 is 60°, then firing angle of conv-2 must be 120°.

Therefore for these firing angles, conv-1 is working as a rectifier and conv-2 as an inverter.

Though the o/p vol at the terminals of both conv 1 & 2 has the same avg value & also has the same polarity, their instantaneous o/p vol waveforms, however are not similar as shown by v_{o1} & v_{o2}.

As a consequence of it, circulating current flows between the two converters.

This circulating current is limited by the reactor.

If the load current is to be reversed, the role of two converters is interchanged.

The normal delay period of 10 to 20 msec, as required in non-circulating operation, is not needed here.

This makes the dual converter with circulating current operation faster.

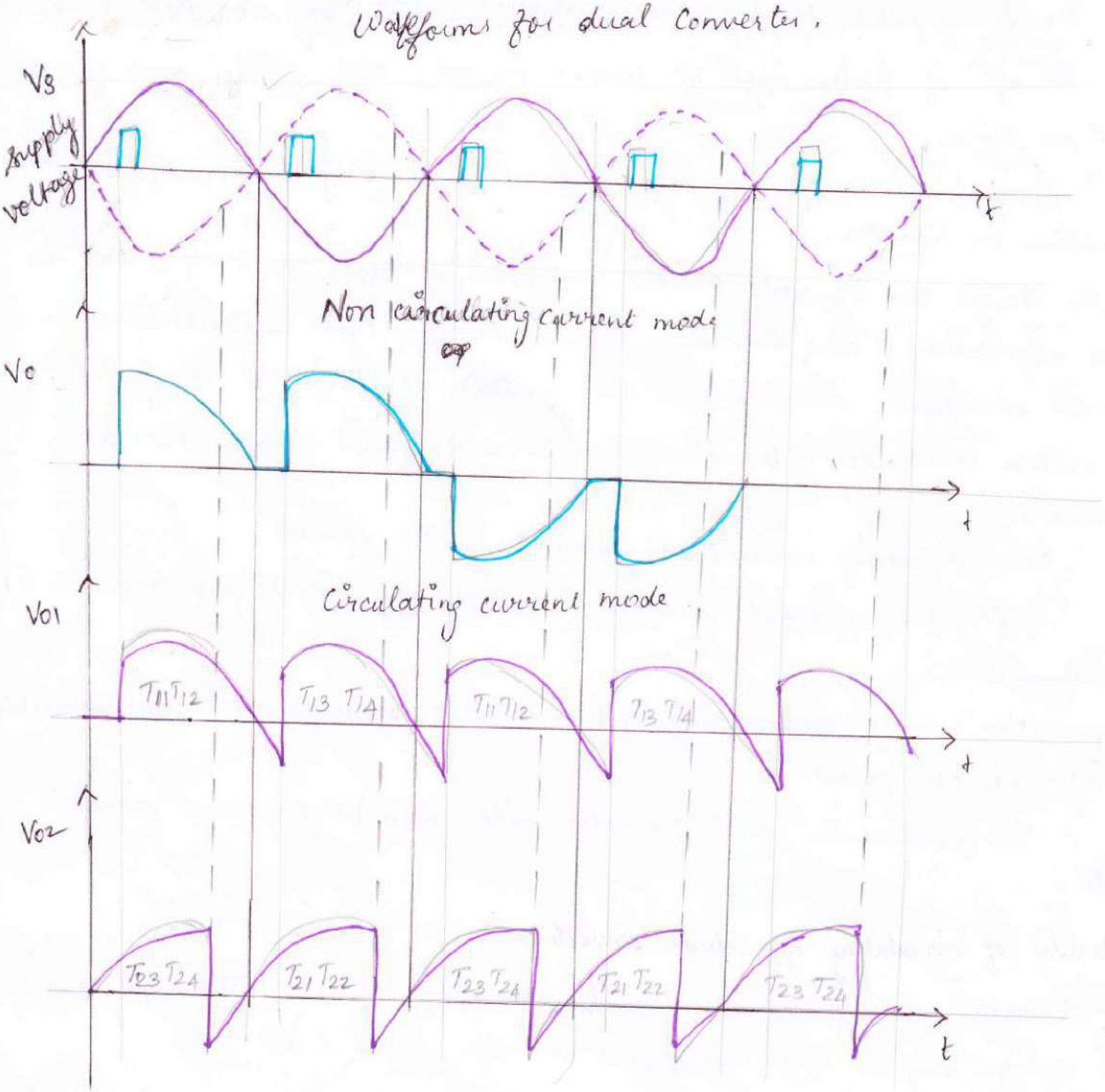
Disadv of circulating type dual converter.

i) A reactor is required to limit the circulating current. The size & cost of this reactor may be quite significant at high power levels.

ii) Circulating current gives rise to more losses in the converters, hence the efficiency & power factor are low.

iii) As the converters have to handle load aswell as circulating currents, the thyristors for the two converters are rated for higher currents.

Waveforms for dual Converter.



Average load current (I_o)

$$I_{dc} \text{ (or) } I_o = \frac{V_o}{R}$$

$$\boxed{V_o = \frac{V_m}{\pi R}(1+\cos\alpha)}$$

RMS load voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \, d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\int_{\alpha}^{\pi} \frac{1-\cos 2\omega t}{2} \, d\omega t\right]^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi}\right\}^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\pi - \frac{\sin 2\pi}{2} - \left(\alpha - \frac{\sin 2\alpha}{2}\right)\right]\right\}^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}$$

RMS load current (I_{rms})

$$I_{rms} = \frac{V_{rms}}{R}$$

$$\boxed{I_{rms} = \frac{V_m}{R\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}}$$

UNIT - IV INVERTERS AND CYCLOCONVERTER.

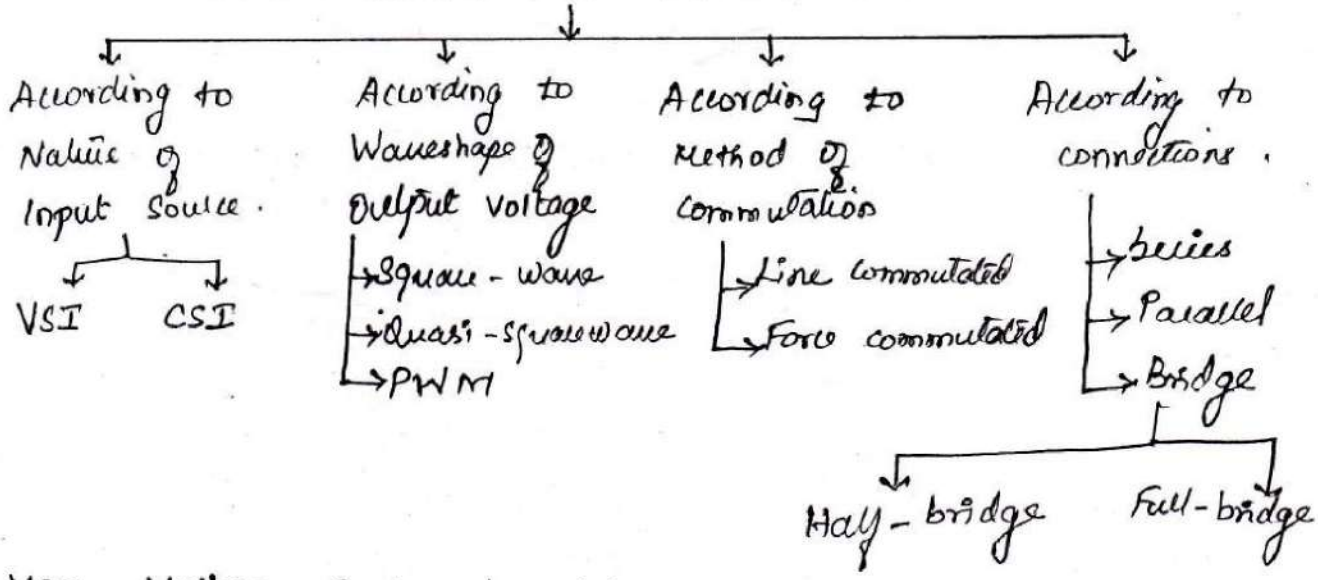
INTRODUCTION.

The d.c to a.c power converters are known as inverters. An inverter is a circuit which converts a d.c. power into an a.c power at desired output voltage and frequency.

APPLICATIONS OF INVERTERS.

1. Variable speed a.c motor drives.
2. Induction heating.
3. Aircraft power supplies.
4. Uninterruptible power supplies (UPS)
5. High Voltage d.c transmission lines.
6. Battery - vehicle drives
7. Regulated voltage and frequency power supplies.

CLASSIFICATION OF INVERTERS.



VSI - Voltage source Inverters

The input to the inverter is provided by a ripple free dc voltage source.

CSI - Current Source Inverters.

The voltage is first converted into a current source and then used to supply the power to the inverter.

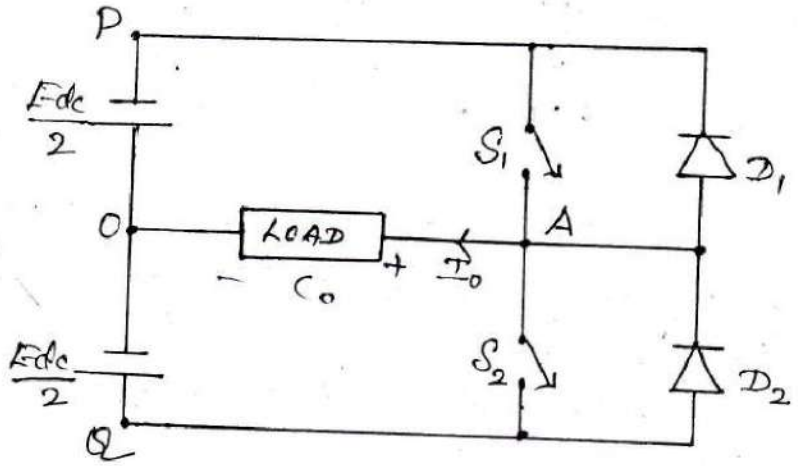
Line commutated Inverters.

In case of a.c circuits, a.c. line voltage is available across the device. When the current in the SCR goes through a natural zero, the device is turned-off. The process is known as natural commutation process and the inverters based on this principle are known as line commutated inverters.

Forced Commutated Inverters.

In case of d.c. circuits, since the supply voltage does not go through the zero point, some external source is required to commutate the device. This process is known as the forced commutation process and the inverters based on this principle are called as forced commutated inverters.

SINGLE PHASE HALF-BRIDGE VOLTAGE SOURCE INVERTERS:



Half-bridge Inverter.

Switches S_1 and S_2 are the gate commutated devices such as power BJTs, MOSFETs, GTO, IGBT, MCT etc. When closed these switches conducts and current flows in the direction of arrow.

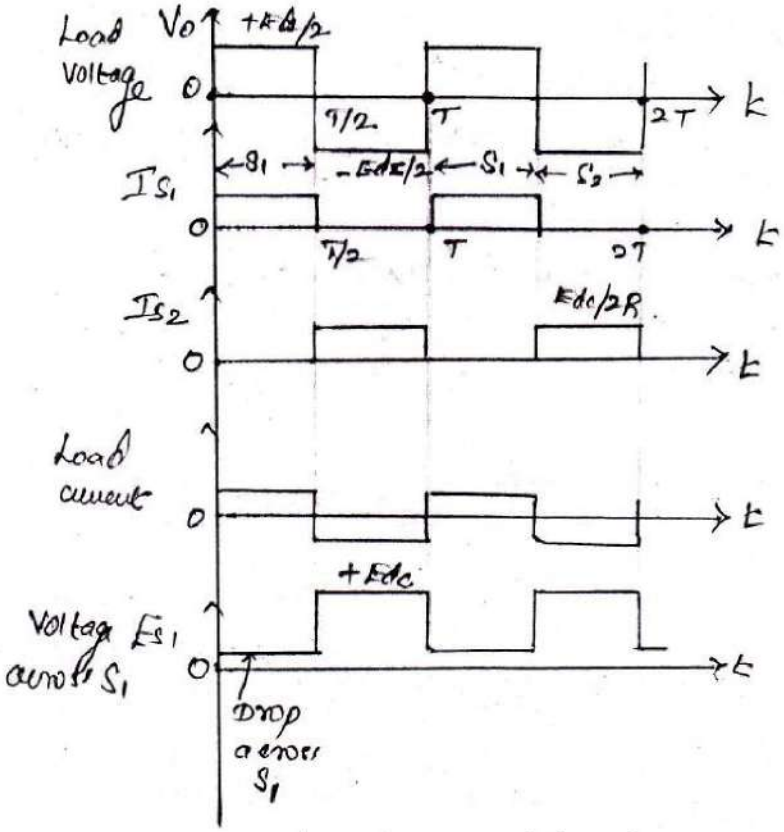
Operation with Resistive load.

The operation of the circuit can be divided into two periods.

i) Period-I, where switch S_1 is conducting from $0 \leq t \leq \frac{T}{2}$

and ii) Period-II, where switch S_2 is conducting from $\frac{T}{2} \leq t \leq T$

where $T = \frac{1}{f}$ and f is the frequency of the output voltage



Voltage and Current Waveforms.

i) RMS Output voltage

The average value of the output voltage is given by

$$E_{o(av)} = \frac{1}{2\pi} \int_0^{2\pi} e_o(\omega t)\, d\omega t .$$

Now, rms value of the output voltage is given by

$$E_{o(rms)} = \sqrt{\frac{1}{2\pi} \int_0^{\pi/2} e_o^2(\omega t)\, d\omega t .}$$

$$= \sqrt{\frac{4}{2\pi} \int_0^{\pi/2} e_o^2(\omega t)\, d\omega t}$$

$$= \sqrt{\frac{2}{\pi} \int_0^{\pi/2} \left(\frac{E_{dc}}{2}\right)^2 d\omega t}$$

$$= \frac{E_{dc}}{2} .$$

Rms value of a square - wave is equal to its peak - value.

(ii) Instantaneous Output voltage.

The Fourier - series can be found out by using the following equation

$$e_o(\omega t) = \sum_{n=1,2,3,\ldots}^{\infty} C_n \sin(n\omega t + \phi_n)$$

where $C_n = \sqrt{a_n^2 + b_n^2}$ and $\phi_n = \tan^{-1}(a_n/b_n)$

and $a_n = \frac{1}{\pi} \int_0^{2\pi} e_o(\omega t) \cos(n\omega t) . d\omega t = 0$ due to square wave symmetry

and $b_n = \frac{1}{\pi} \int_0^{2\pi} e_o(\omega t) . \sin(n\omega t)\, d\omega t .$

Due to quarter-wave symmetry, $b_n = 0$, for all even 'n'

$$\therefore b_n = \frac{4}{\pi} \int_0^{\pi/2} \frac{E_{dc}}{2} \sin(n\omega t)\, d\omega t, \text{ for all odd 'n'.}$$

$$b_n = \frac{2E_{dc}}{n\pi}, \text{ for odd value of } n.$$

$$\therefore C_n = \sqrt{a_n^2 + b_n^2} = \frac{2E_{dc}}{n\pi} \text{ and } \phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) = 0.$$

Therefore, the instantaneous output voltage of a half-bridge inverter can be expressed in fourier-series form as

$$e_0(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{2}{\pi} \frac{E_{dc}}{n} \sin(n\omega t)$$

$= 0$, for $n = 2, 4, \ldots$ (even values of n)

The n^{th} harmonic-component is given by

$$e_0(n) = \frac{C_n}{\sqrt{2}} = \frac{2E_{dc}}{n\pi \cdot \sqrt{2}} = \frac{\sqrt{2}}{n} \frac{E_{dc}}{n} \quad \text{for } n = 1, 3, 5 \ldots\ldots$$

Rms value of fundamental components is obtained by substituting $n = 1$ in above equation,

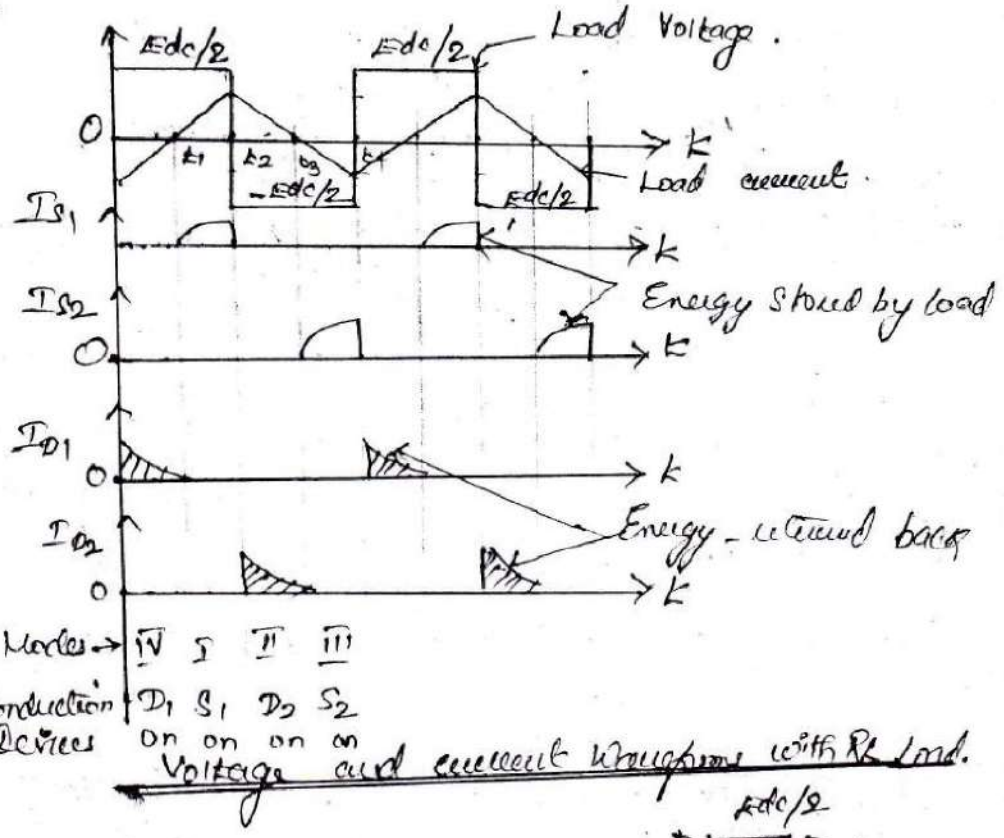
$$\therefore E_{1(max)} = \frac{\sqrt{2}}{\pi} E_{dc} = 0.45\, E_{dc}.$$

Operation with RL Load.

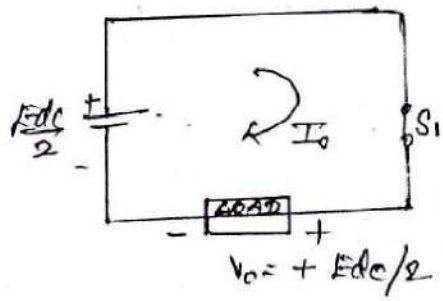
With an inductive-load, the output voltage waveform is similar to that with a resistive-load, however the load-current cannot change immediately with the output voltage.

The operation of half-bridge inverter with RL Load is divided into four distinct modes.

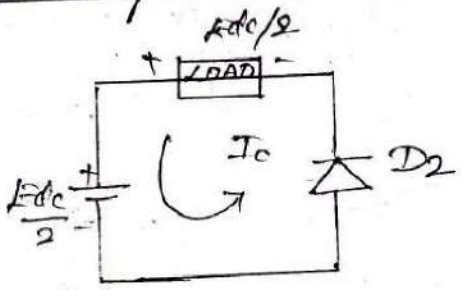
(i) Mode 1 ($t_1 < t < t_2$)
(ii) Mode 2 ($t_2 < t < t_3$)
(iii) Mode 3 ($t_3 < t < t_4$)
(iv) Mode 4 ($t_0 < t < t_1$)



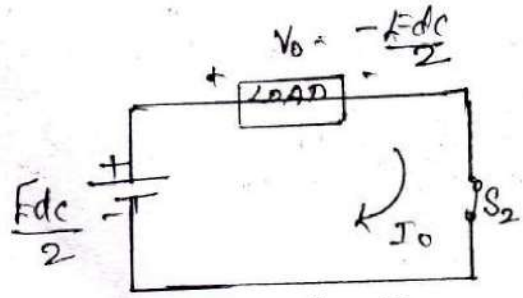
Voltage and current waveforms with RL Load.



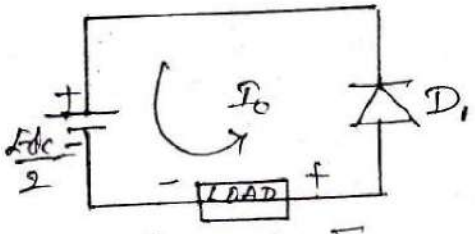
(a) Mode - I



(b) Mode - II



(c) Mode - III



(d) Mode - IV

Mode - II ($t_2 < t < t_3$).

Both the switches S_1 and S_2 are turned-off at instant t_2. Due to inductive nature of the load, the load current does not reduce to zero instantaneously.

There is a self-induced voltage across the load which maintains the flow of current in the same-direction. The polarity of this voltage is exactly opposite to that in mode-1. The output voltage becomes $-E_{dc}$, but the load current continues to flow in the same direction, through D_3 and D_4

Thus, in this mode, the stored energy in the load inductance is returned back to the source.

Load current decreases exponentially and goes to 0 at instant t_3 when all the energy stored in the load is returned back to supply. D_3 and D_4 are turned-off at t_3.

Mode - III ($t_3 < t < t_4$)

Switches S_3 and S_4 are turned-ON simultaneously at instant t_3.

Load voltage remains negative ($-E_{dc}$) but the direction of load current will reverse. The current increases exponentially in the other direction and the load again stores the energy.

Mode - IV ($t_0 < t < t_1$).

Switches S_3 and S_4 are turned-off at instant t_0. The load inductance tries to maintain the load current in the same direction by inducing the positive-load voltage.

This will forward-bias the diodes D_1 and D_2. The load energy is returned back to the input dc supply. The load voltage becomes $e_0 = +E_{dc}$ but the load current remains negative and

decreases exponentially towards 0. At t_1, the load current goes to zero and switches S_1 and S_2 can be turned-on again. The conduction period with a very highly inductive load, will be T/4 or 90° for all the switches as well as the diodes.

The conduction period of switches will increase towards $\frac{T}{2}$ or 180° with increase in the load power factor.

(i) RMS output voltage

$$E_{rms} = \left[\frac{2}{T/2}\int_0^{T/2} E^2\,dt\right]^{1/2}$$

$$= Edc$$

(ii) The instantaneous output voltage can be expressed in fourier series as

$$e_o(\omega t) = \sum_{n=1,3,5\cdots}^{\infty} \frac{4Edc}{n\pi} \sin n\omega t.$$

The output voltage waveform contains only the odd harmonic components.

(iii) for n=1, the rms value of the fundamental component

$$E_1(rms) = \frac{4Edc}{\sqrt{2}\cdot\pi} = 0.9\,Edc.$$

(iv) For RL Load, the equation for the instantaneous current i_o,

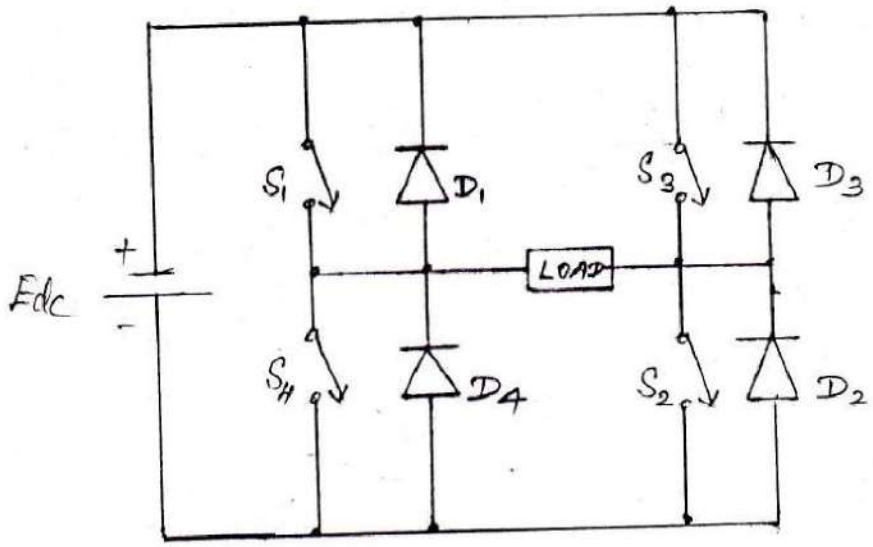
$$i_o(t) = \sum_{n=1,3,5\cdots}^{\infty} \frac{4Edc}{n\pi\sqrt{R^2+(n\omega L)^2}} \sin(n\omega t - \theta_n).$$

where $Z_n = \sqrt{R^2+(n\omega L)^2}$ is the impedance offered by the load to the n^{th} harmonic component and $\frac{4Edc}{n\pi}$ is the peak amplitude of n^{th} harmonic voltage and $\theta_n = \tan^{-1}(n\omega L/R)$.

SINGLE PHASE FULL BRIDGE INVERTER.

The inverter uses two pairs of controlled switches (S_1S_2 and S_3S_4) and two pairs of diodes (D_1D_2 and D_3D_4).

In order to develop a positive voltage ($+E_0$) across the load, switches S_1 and S_2 are turned-on simultaneously whereas to have a negative voltage ($-E_0$) across the load, we need to turn-on the switches S_3 and S_4. Diodes D_1, D_2, D_3 and D_4 are known as the feedback diodes.



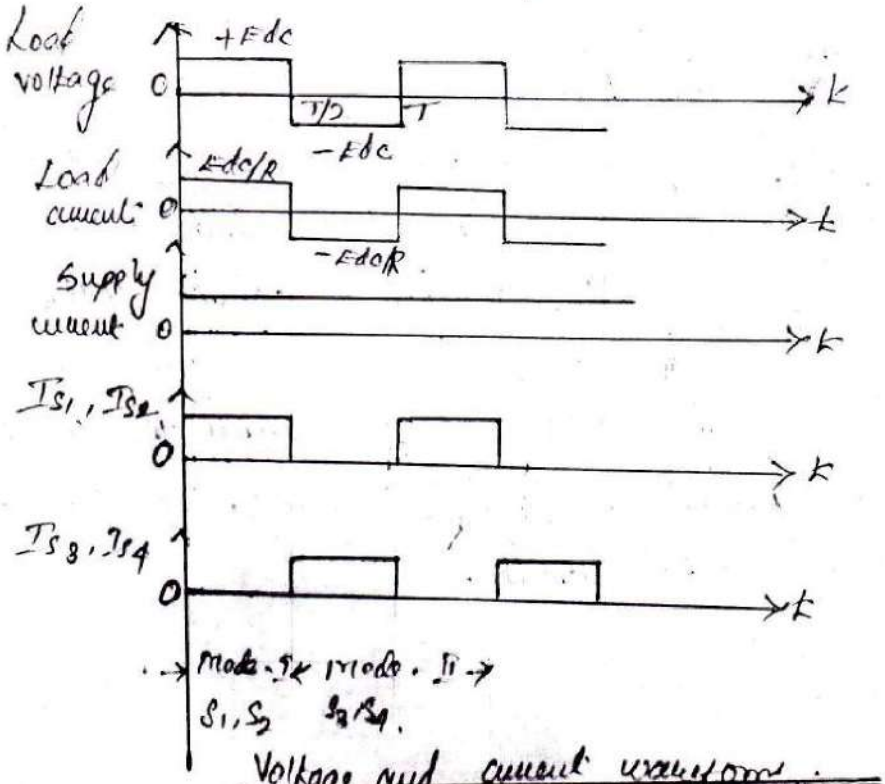
1φ full bridge inverter.

Operation with Resistive Load.

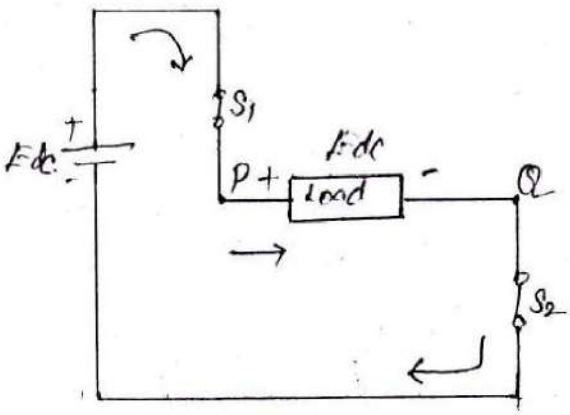
The bridge-inverter operates in two-modes in one-cycle of the output.

mode-I ($0 < t < T/2$).

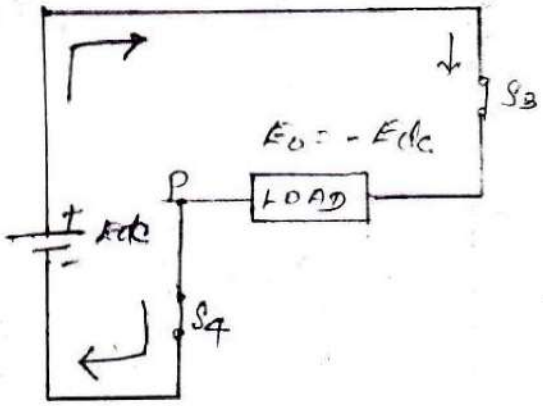
In this mode, switches S_1 and S_2 conducts simultaneously. The load voltage is $+E_{dc}$ and load current flows from P to Q. At $t = T/2$, S_1 and S_2 are turned-off and S_3 and S_4 are turned-on.



Voltage and current waveforms.



(a) Mode - I



(b) Mode - IV

Equivalent circuit.

Mode - II ($T/2 < t < T$).

At $t = T/2$, Switches S_3 and S_4 are turned - ON and S_1 and S_2 are turned - off. The load voltage is $-E_{dc}$ and load current flows from Q to P. As the load is resistive, it

does not store any energy.

(i) Rms output voltage, $E_{o(rms)} = E_{dc}$.

(ii) Fourier series, $e_o(\omega t) = \sum_{n=1,3,5\ldots}^{\infty} (4E_{dc}/n\pi) \cdot \sin(n\omega t)$.

(iii) Fundamental Output voltage, $E_{o(fund)} = \frac{2\sqrt{2}}{\pi} \cdot E_{dc}$.

(iv) nth harmonic voltage $E_{o(n)} = \frac{E_{o(fund)}}{n}$.

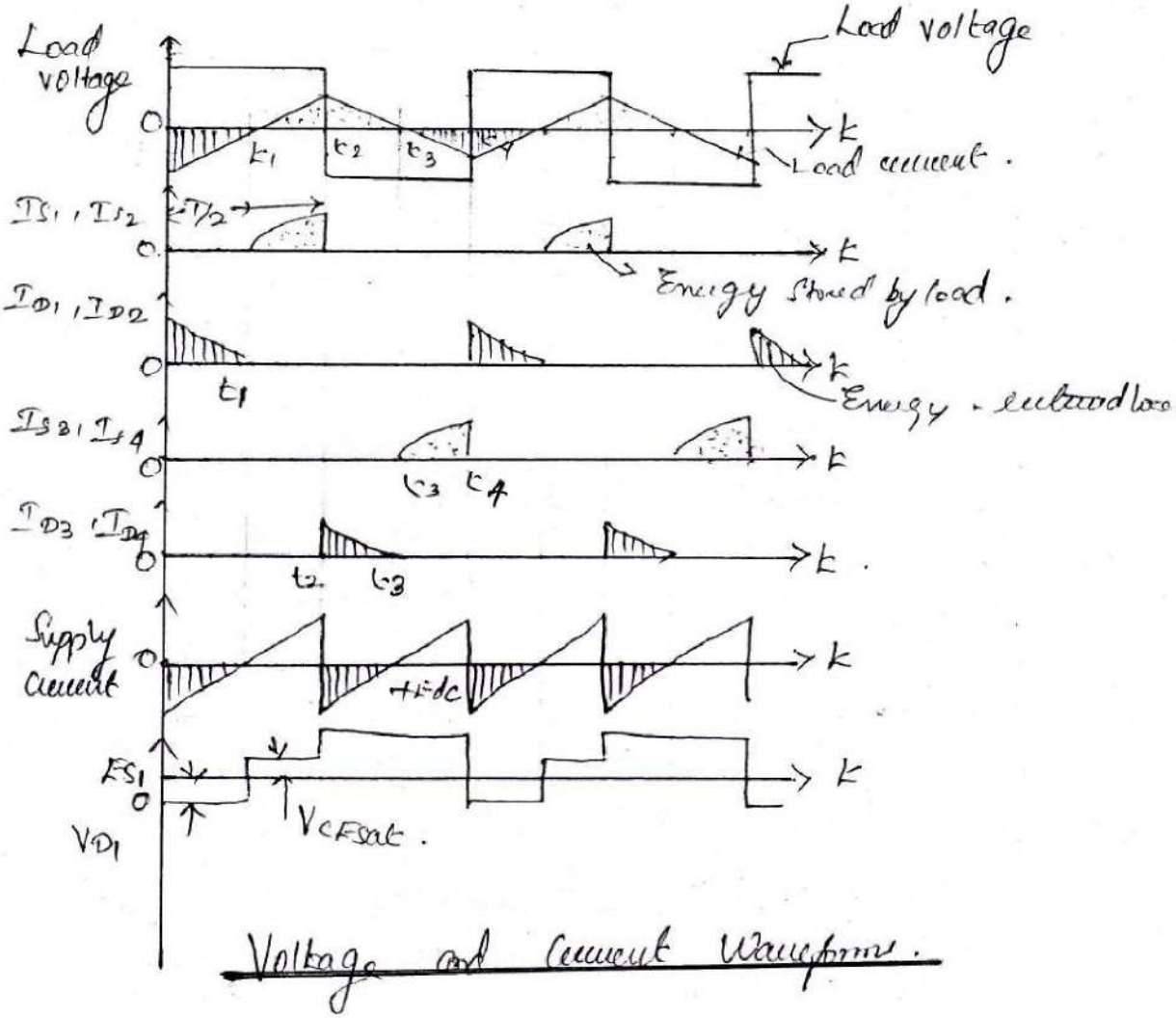
(v) Transistor (switch) ratings,

$$V_{CE0} \geq E_{dc}, \quad I_{T(av)} = \frac{E_{dc}}{R}$$

$$I_{T(rms)} = \frac{E_{dc}}{\sqrt{2} \cdot R}, \quad I_{T(peak)} = \frac{E_{dc}}{R}.$$

Operation with RL Load.

The operation of the circuit is explained in four modes.

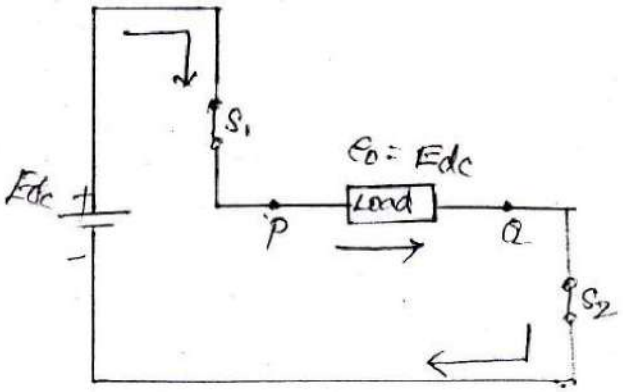


Voltage and current Waveforms.

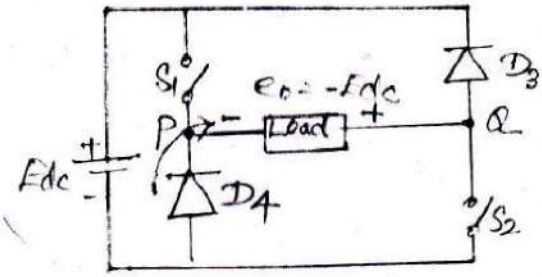
Mode - 1 ($t_1 < t < t_2$)

At instant t_1, the switch S_1 and S_2 are turned - on. Point P gets connected to positive point of dc source E_{dc} through S_1 and point Q gets connected to negative point of input supply.

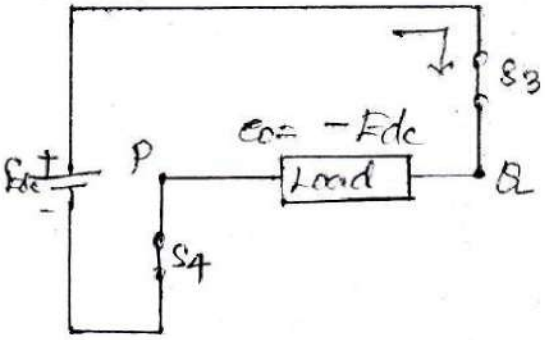
The output voltage, $e_o = +E_{dc}$. The instantaneous current through S_1 and S_2 is equal to the instantaneous load current. During this interval, energy is stored in inductive load.



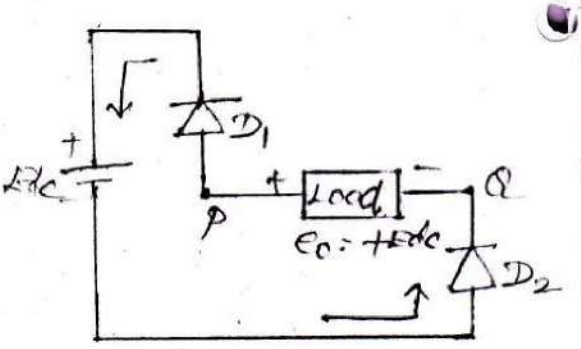
(a) Mode I ($t_1 < t < t_2$)



(b) Mode II ($t_2 < t < t_3$)



(c) Mode - III ($t_3 < t < t_4$).



(d) Mode - IV ($t_4 < t < t_1$)

Equivalent circuits.

THREE PHASE INVERTERS.

Three-phase inverters are used for high-power application such as ac motor drives, induction heating, uninterruptible power supplies.

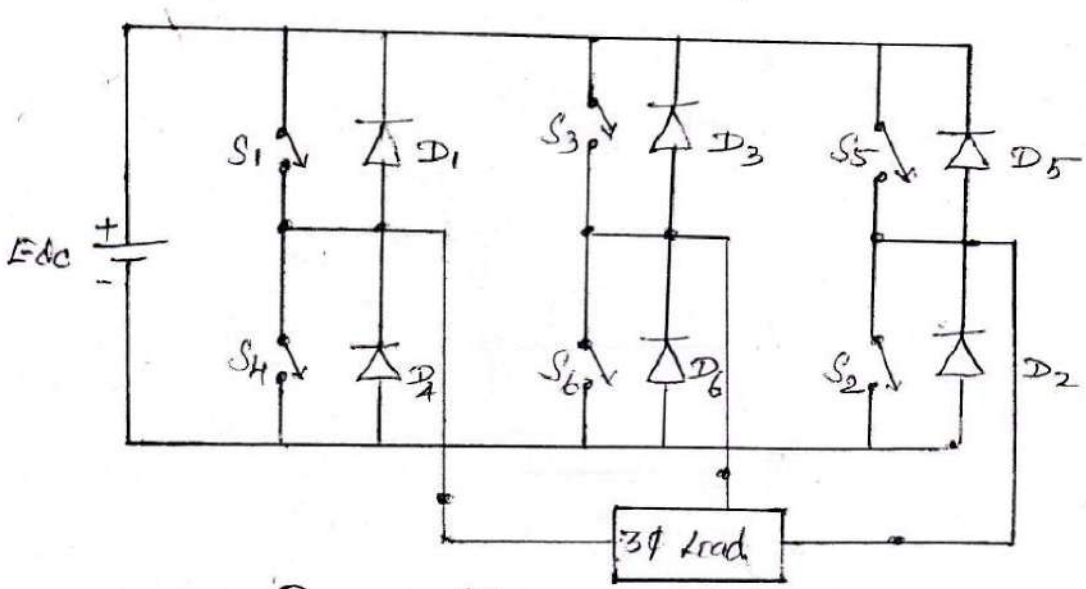
A three phase inverter circuit changes DC input voltage to a three-phase variable frequency, variable voltage output.

The circuit consists of six power-switches with six associated freewheeling diodes. The switches are opened and closed periodically in the proper sequence to produce the desired output waveform. The rate of switching determines the output frequency of the inverter.

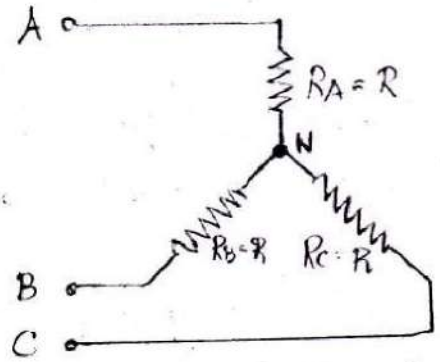
Basically, there are two possible schemes of gating the devices. In one scheme, each device (switch) conducts for 180° and in the other scheme, each device conducts for 120°.

180° - Conduction Mode with Resistive load.

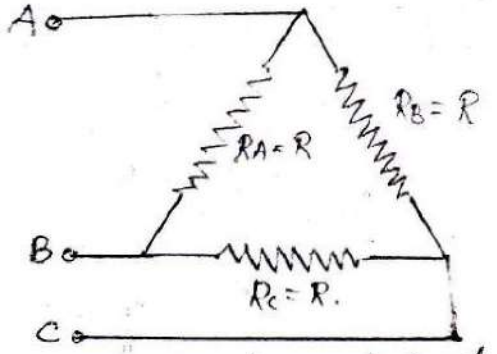
In this control scheme, each switch conducts for a period of 180° or half-cycle electrical. Switches are triggered in sequence of their numbers with an interval of 60°.



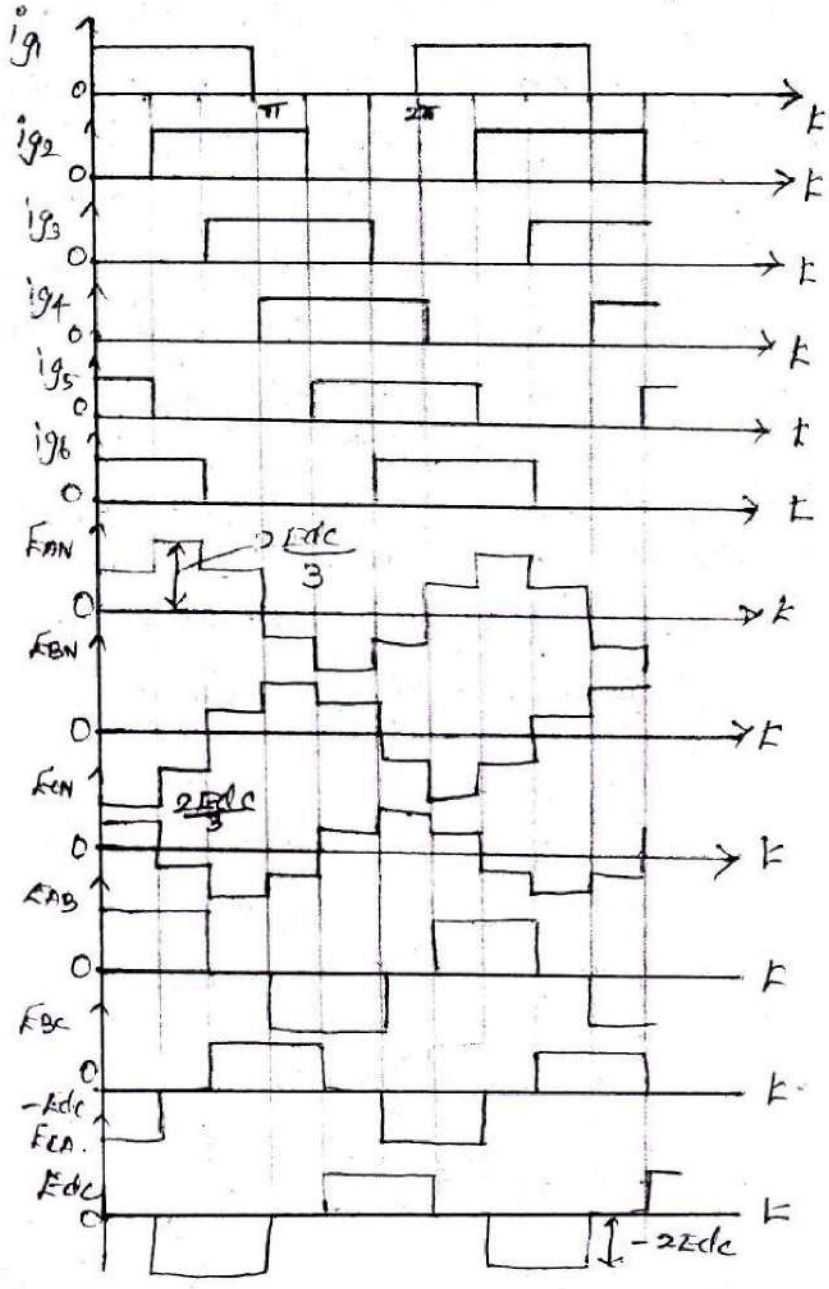
Power circuit.



Star - connected load.



Delta - Connected load



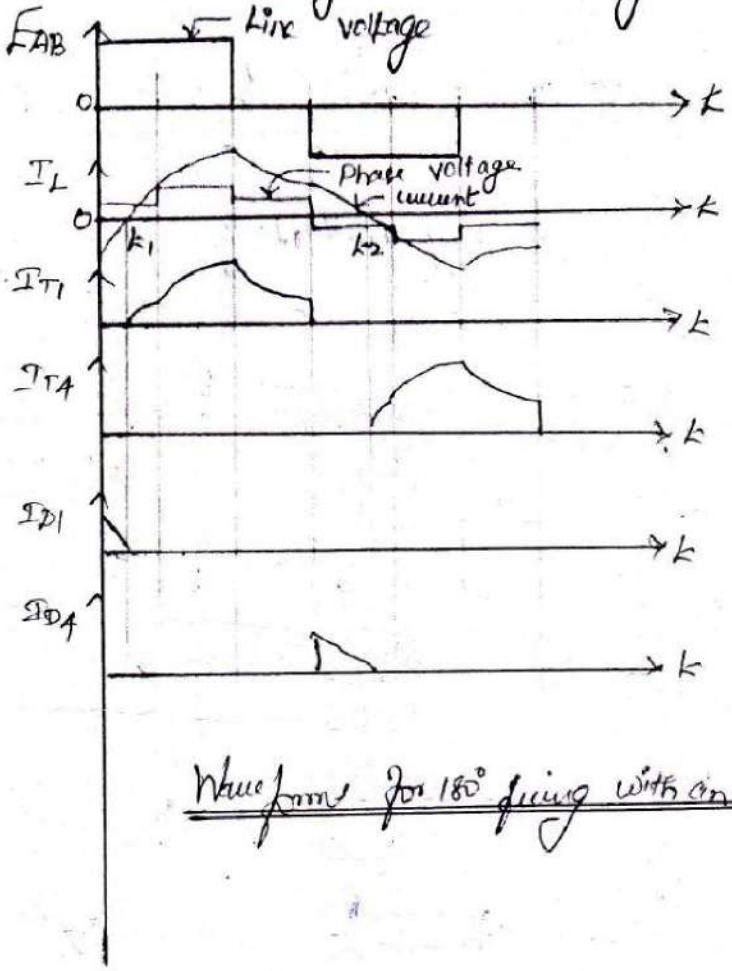
Voltage Waveforms for 180° conduction.

Operation Table.

Sl.NO	Interval	Device conducting	Incoming Device	Outgoing device.
1.	I	5, 6, 1	1	4
2.	II	6, 1, 2	2	5
3.	III	1, 2, 3	3	6
4.	IV	2, 3, 4	4	1
5.	V	3, 4, 5	5	2
6.	VI	4, 5, 6	6	3

180° Conduction Mode with RL Load.

If the load is inductive, then the current in each arm of the load will be delayed to its voltage.



Waveforms for 180° firing with an RL load.

When switch S_1 is triggered, S_4 is turned-off. but, because the load current cannot reverse, the only path for this current is through diode D_1.

Hence the load phase is connected to the positive end of the dc source but, until the load current reverses at t_1, switch S_1 will not take up conduction.

(i) Phase Voltage, $E_{AN} = \frac{E_{AB}}{\sqrt{3}}$ with a delay of 30°.

(ii) Line current, I_L, for an RL Load is given by

$$I_L = \sum_{n=1,3,5}^{\infty} \left[\frac{4 E_{dc}}{\sqrt{3} \cdot n\pi \sqrt{R^2 + (n\omega L)^2}} \cdot \cos\frac{n\pi}{6} \right] \sin(\omega t - \theta_n)$$

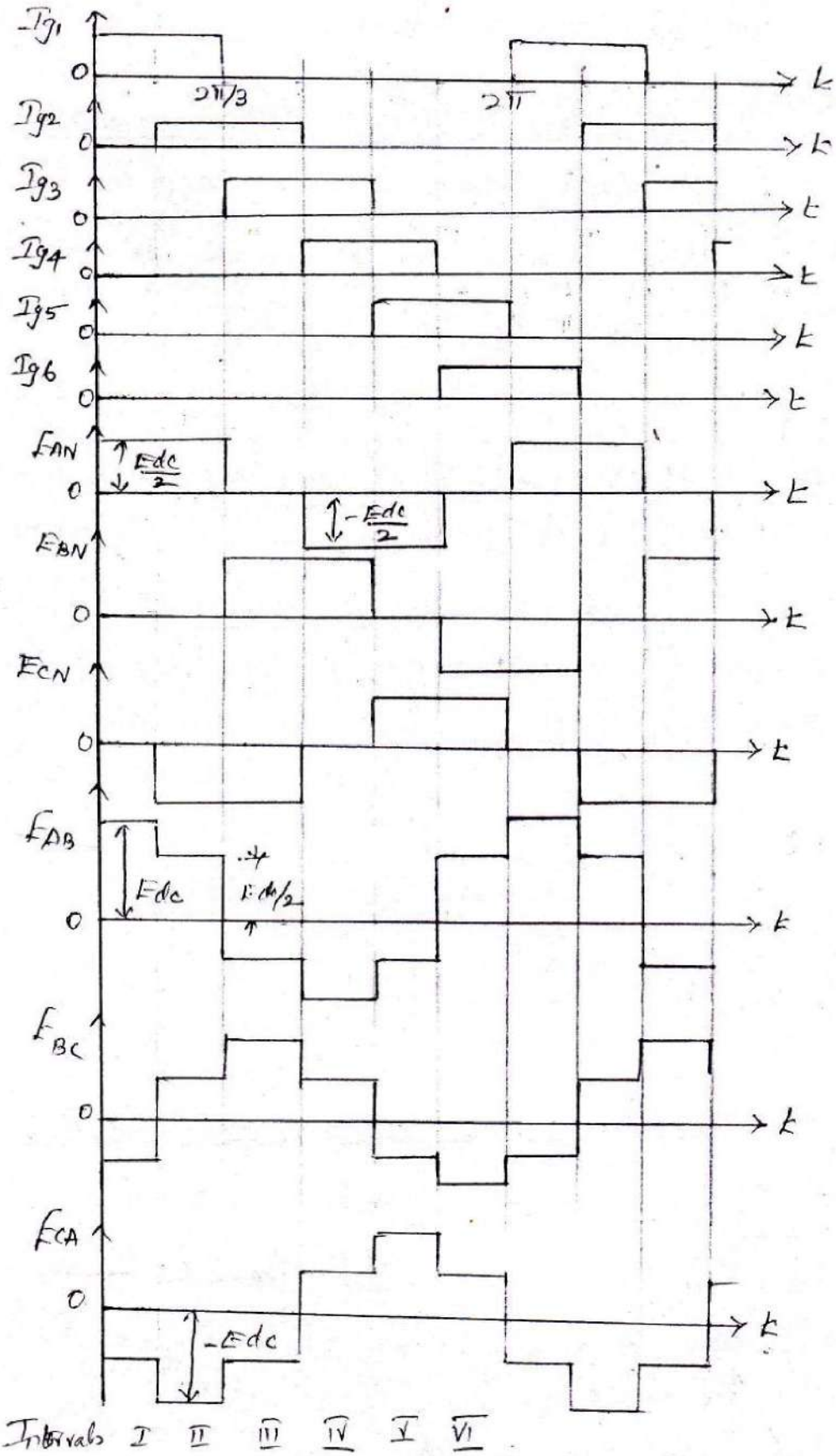
where $\theta_n = \tan^{-1}\left(\frac{n\omega L}{R}\right)$

120° Conduction Mode with Resistive Load.

In this type of conduction mode, each switch conducts for 120°. At any instant of time, only two switches remain on.

Operation Table.

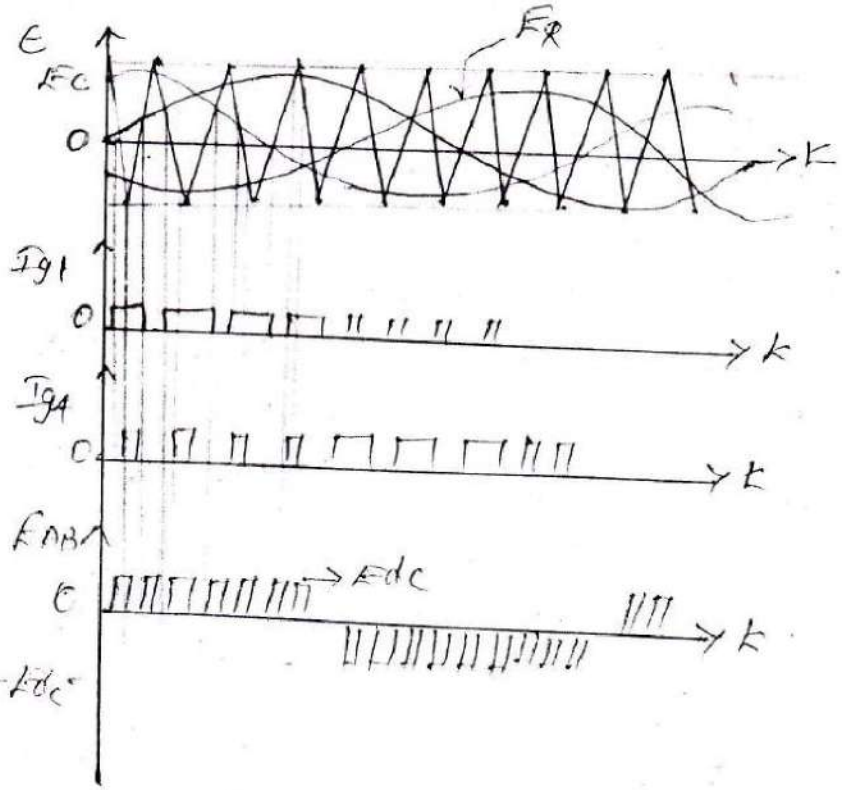
Sl. No	Interval	conducting devices	Incoming device	Outgoing device.
1.	I	S_6, S_1	S_1	S_5
2.	II	S_1, S_2	S_2	S_6
3.	III	S_2, S_3	S_3	S_1
4.	IV	S_3, S_4	S_4	S_2
5.	V	S_4, S_5	S_5	S_3
6.	VI	S_5, S_6	S_6	S_4.



Gating Signals and Voltage waveform for 120° conduction.

VOLTAGE CONTROL OF THREE-PHASE INVERTERS.

A three phase inverter may be considered as three single-phase inverters and the output of each single-phase inverter is shifted by 120°.



Sinusoidal pulse-width modulation for 3φ Inverters

A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. The output voltage, is generated by eliminating the condition that two switching devices in the same arm cannot conduct at the same time.

VOLTAGE CONTROL OF SINGLE-PHASE INVERTERS.

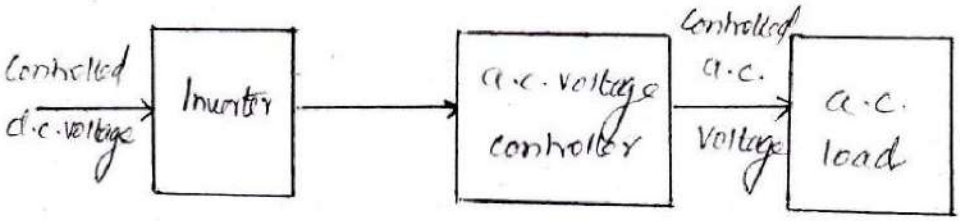
The various methods for the control of output voltage of inverters are

i) External control of a.c output voltage.
ii) External control of d.c input voltage.
iii) Internal control of inverter.

The first two methods require the use of peripheral components, whereas the third method requires no peripheral components.

(i) External control of a.c. Output Voltage.

In this type of control, an a.c. voltage controller is inserted between the output terminals of inverter and the load terminals.

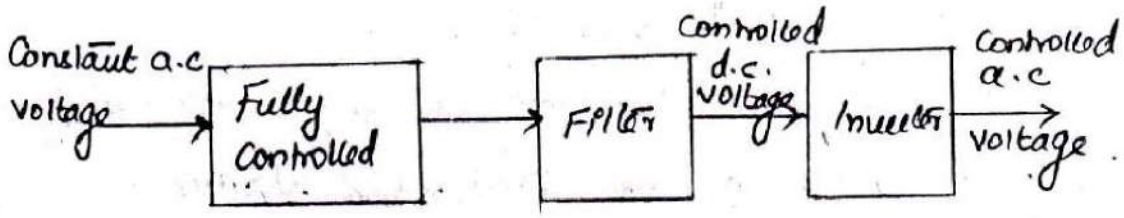


Through the firing angle control of a.c voltage controller, the voltage input to the a.c load is regulated. This method gives rise to higher harmonic content in the output voltage, particularly when the output voltage from the a.c voltage controller is at low level.

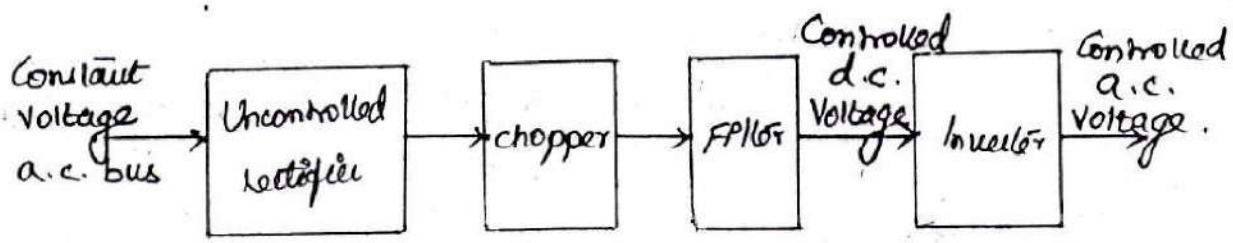
Therefore this method is rarely employed except for low power applications.

(ii) External Control of D.C Input Voltage.

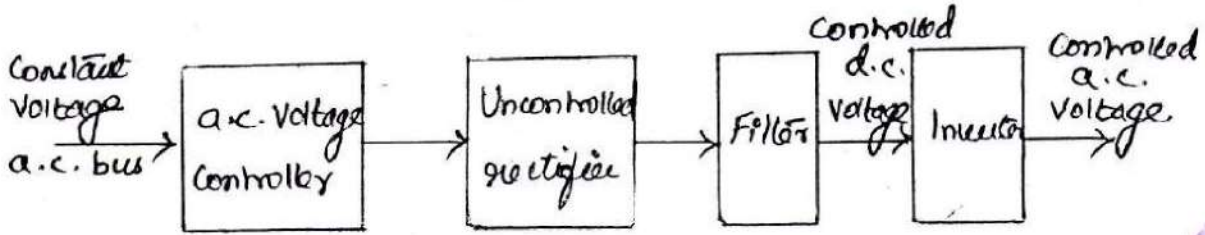
When the available voltage source is a.c, then, d.c voltage input to the inverter is controlled through a fully-controlled rectifier.



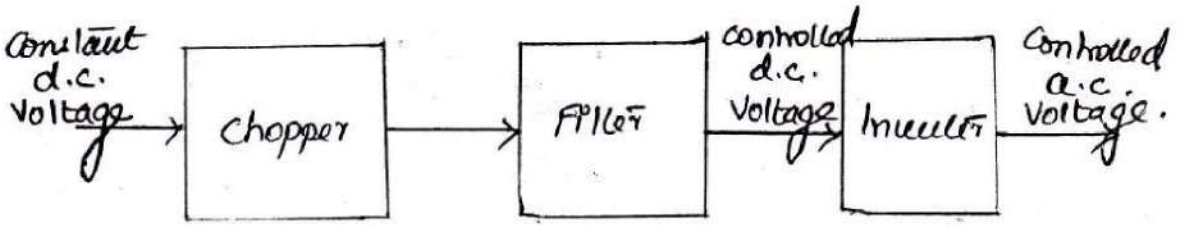
(a)



(b)



(c)



(d)

Voltage control by Controlling d.c. I/P voltage.

(iii) Internal control of Inverter.

Inverter output voltage can also be adjusted by exercising a control within the inverter itself. The two possible ways are

1. Series inverter control and
2. Pulse-width modulation control.

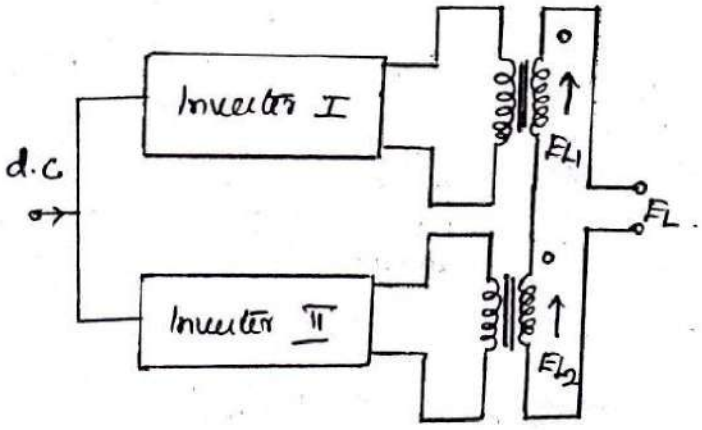
1. Series Inverter control.

This method of voltage control involves the use of two or more inverters in series.

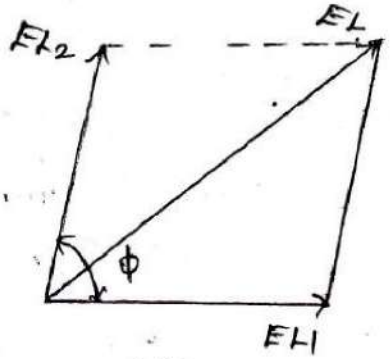
The inverter output is fed to two transformers whose secondaries are connected in series. Phasor sum of the two voltages E_{L1}, E_{L2} gives the resultant voltage E_L.

The voltage E_L is given by

$$E_L = \left[E_{L1}^2 + E_{L2}^2 + 2E_{L1}E_{L2}\cos\theta\right]^{1/2}$$



(a).



(b)

Internal control of inverters by their series connection.

2. Pulse - width Modulation Control.

The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters.

In this method, a fixed d.c. input voltage is supplied to the inverter and a controlled a.c. output voltage is obtained by adjusting the ON and OFF periods of the inverter devices.

Advantages.

1. The output voltage control can be obtained without any additional components.

2. With this type of control, lower order harmonics can be eliminated or minimised along with its output voltage control. The following requirements are minimised as higher order harmonics can be filtered easily.

PWM TECHNIQUES.

The commonly used PWM control techniques are

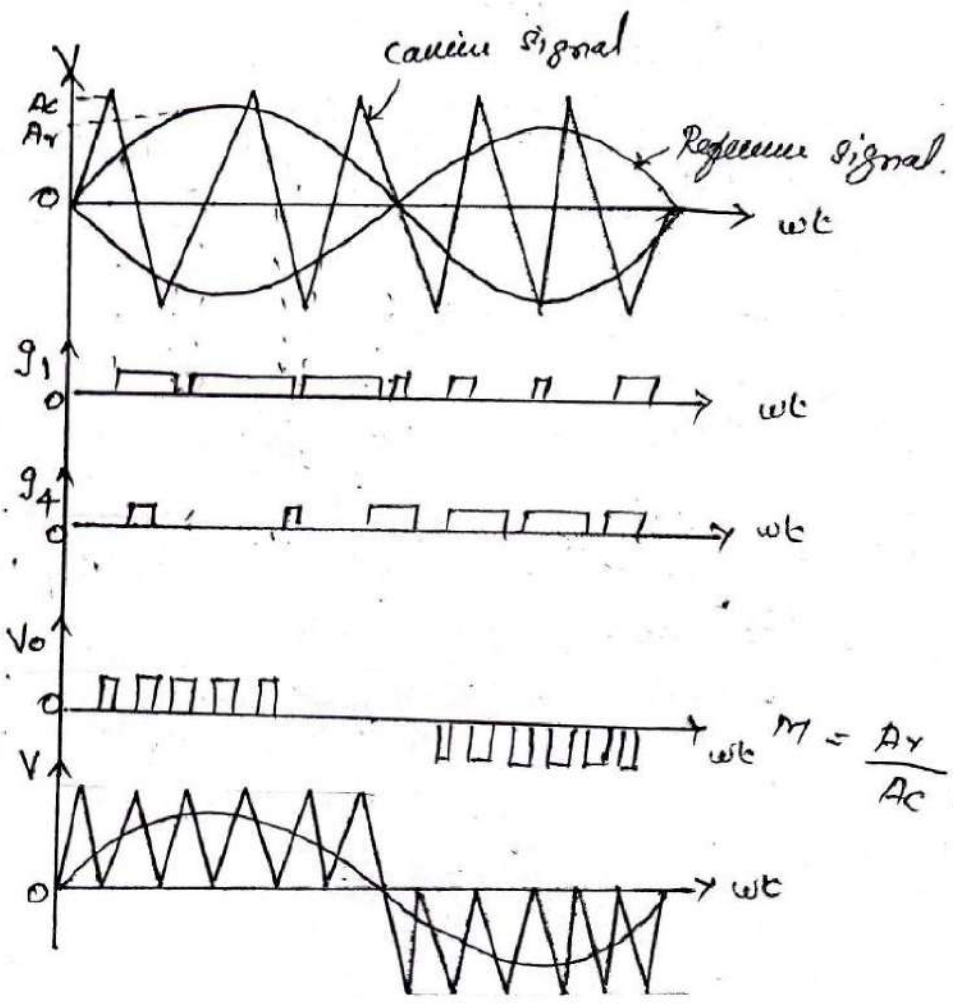
(i) Single - pulse width modulation
(ii) Multiple - pulse width modulation
(iii) Sinusoidal - pulse width modulation
(iv) Modified sinusoidal pulse - width modulation.
(v) Phase - displacement control.

(i) Sinusoidal pulse-width modulation.

The width of each pulse is varied in proportion to the amplitude of a sinewave evaluated at the centre of the same pulse.

The DF and LOH are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c. This sinusoidal pulse-width modulation (SPWM) is commonly used in industrial applications.

The frequency of reference signal f_r determines the inverter output frequency f_o and its peak amplitude A_r controls the modulation index M and thereby in turn the rms output voltage V_o.



$V_r = V_r \sin \omega t$, is reference signal.

$V_o = V_s (g_1 - g_4)$, is output voltage.

∴ The rms output voltage is

$$V_o = V_s \left(\sum_{m=1}^{2p} \frac{\delta_m}{\pi} \right)^{1/2}$$

Fourier coefficient of output voltage is

$$B_n = \sum_{m=1}^{2p} \frac{4 V_s}{n\pi} \sin \frac{n\delta_m}{4} \left[\sin n\left(\alpha_m + \frac{3\delta_m}{4} \right) - \sin n\left(\pi + \alpha_m + \frac{\delta_m}{4} \right) \right]$$

for $n = 1, 3, 5 \ldots\ldots$

The m^{th} time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = t_x + m\frac{T_s}{2}$$

where t_x can be solved from

$$1 - \frac{2t}{T_s} = m \sin \left[\omega \left(t_x + \frac{mT_s}{2} \right) \right] \text{ for } m = 1, 3 \ldots\ldots 2p$$

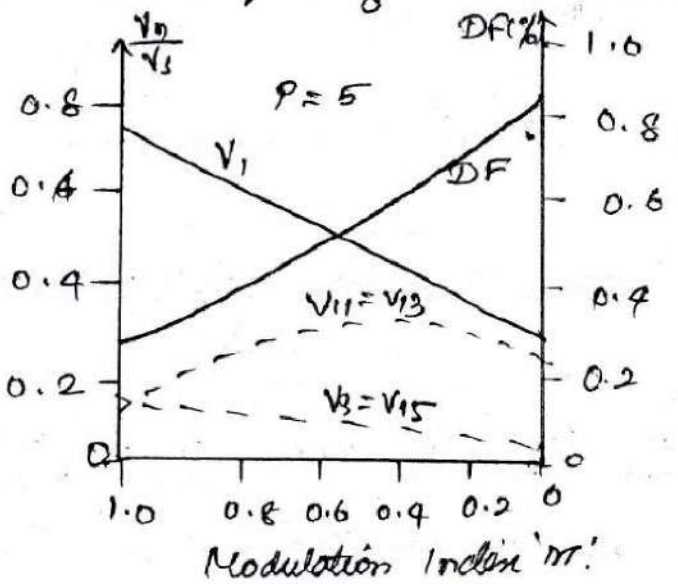
$$\frac{2t}{T_s} = m \sin \left[\omega \left(t_x + \frac{mT_s}{2} \right) \right] \text{ for } m = 2, 4, \ldots 2p.$$

where $T_s = T/2(p+1)$.

The width of the nth pulse d_n (or pulse angle δ_n) can be found from

$$d_n = \frac{\delta_n}{\omega} = t_{n+1} - t_n.$$

Harmonic profile of sinusoidal pulse-width modulation.



The output voltage of an inverter contains harmonics. The PWM pushes the harmonics into a high-frequency range around the switching frequency f_c and its multiples, i.e around harmonics mf, $2mf$, $3mf$.....

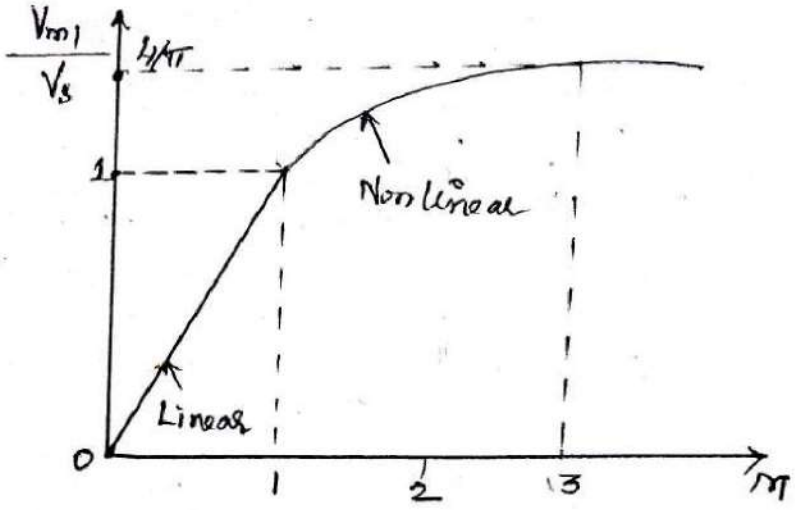
The frequencies at which the voltage harmonics occur can be related by

$$f_n = (j m_f \pm k) f_c$$

where the n^{th} harmonic equals the k^{th} sideband of j^{th} times the frequency to modulation ratio m_f.

$$n = j m_f \pm k.$$

$$= 2jp \pm k \quad \text{for } j = 1, 2, 3 \ldots \text{ and } k = 1, 3, 5 \ldots$$



Peak fundamental Output voltage versus modulation index :

(ii) Modified Sinusoidal Pulse - Width Modulation.

The characteristics of a sine wave and the SPWM technique can be modified so that the carrier wave is applied during the first and last 60° intervals per half-cycle (ie 0-60° and 120° to 180°).

The fundamental component is increased and the harmonic characteristics are improved. It reduces the number of switching of power devices and also reduces switching losses.

The n^{th} time t_n and angle α_n of intersection can be determined from

$$t_n = \frac{\alpha_n}{\omega} = t_{n-1} + m\frac{T_s}{2} \quad \text{for } n = 1, 2, 3 \ldots p$$

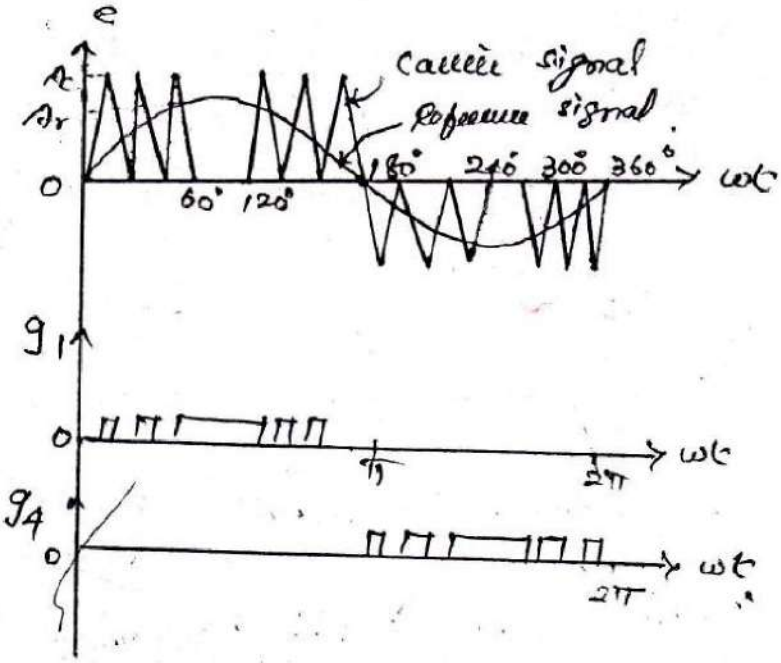
where t_x can be solved from

$$1 - \frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \quad \text{for } m = 1, 3 \cdots p$$

$$\frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \quad \text{for } m = 2, 4 \cdots p$$

The time interval during the last 60° intervals can be found from

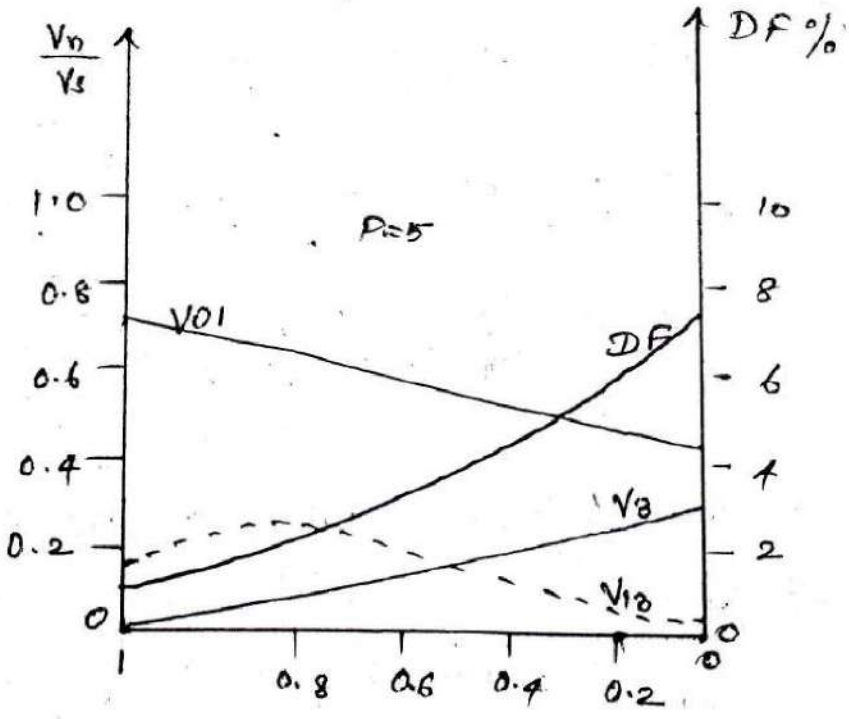
$$t_{m+1} = \frac{\alpha_{m+1}}{\omega} = \frac{T}{2} - t_{2p-m} \quad \text{for } m = p, p+1, \ldots 2p-1$$



Modified Sinusoidal pulse-width modulation

Where $T_s = T/6(p+1)$. The width of the mth pulse d_m (or pulse angle δ_m) can be found from

$$d_m = \frac{\delta_m}{\omega} = t_{m+1} - t_m.$$



Harmonic Profile of modified Sinusoidal pulse-width Modulation:

The number of pulses q in the 60° period is normally related to the frequency ratio, particularly in three-phase inverters, by

$$\frac{f_c}{f_0} = 6q + 3.$$

The instantaneous output voltage is $V_0 = V_s(g_1 - g_4)$.

(iii) Multiple-Pulse-Width Modulation.

The harmonic content can be reduced by using several pulses in each half-cycle of output voltage.

The generation of gating signals for turning on and off of transistors is done by comparing a reference

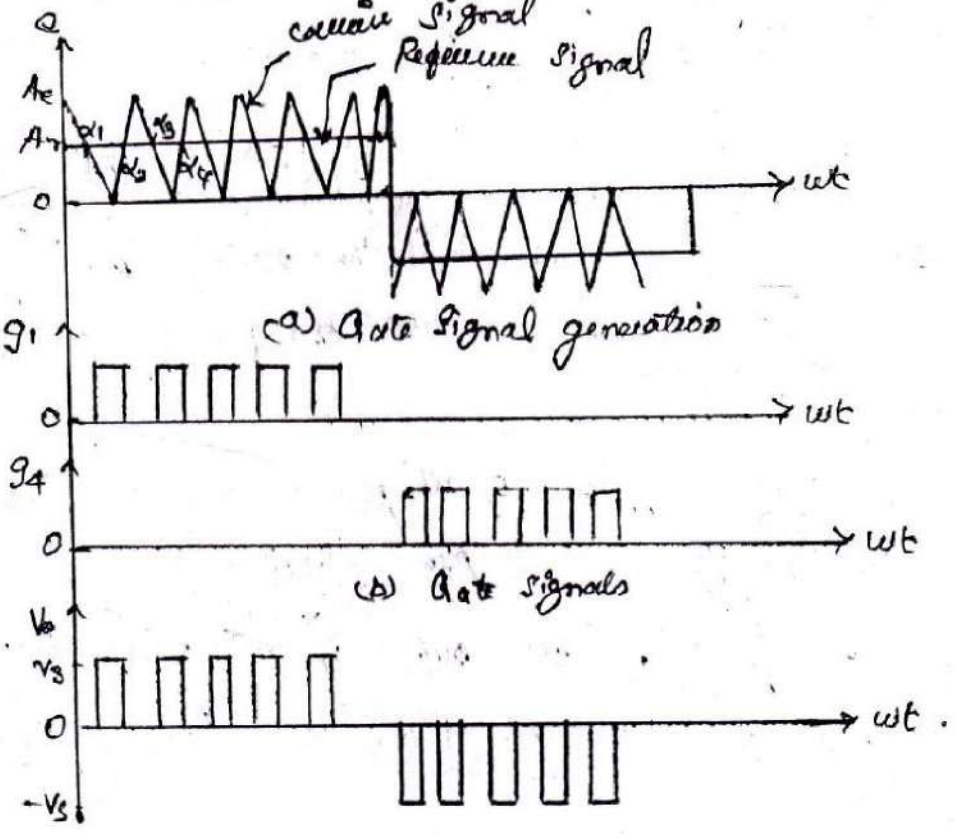
signal with a triangular carrier wave. The frequency of reference signal sets the output frequency f_o and the carrier frequency f_c determines the number of pulses per half-cycle p.

The modulation index controls the output voltage. This type of modulation is also known as uniform pulse-width modulation (UPWM).

The number of pulses per half cycle is found from

$$p = \frac{f_c}{2f_o} = \frac{m_f}{2}$$

where $m_f = \frac{f_c}{f_o}$ is defined as the frequency modulation ratio.



Multiple pulse-width Modulation.

The instantaneous output voltage is $V_o = V_s(g_1 - g_4)$.

If δ is the width of each pulse, the rms output voltage can be found from

$$V_o = \left[\frac{2p}{2\pi}\int_{(\pi/p-\delta)/2}^{(\pi/p+\delta)/2} V_s^2\, d(\omega t)\right]^{1/2} = V_s\sqrt{\frac{p\delta}{\pi}}$$

The variation of the modulation index M from 0 to 1, varies the pulse width of d from 0 to $T/2p$ (0 to π/p) and the rms output voltage V_o from 0 to V_s.

The general form of a Fourier series for the instantaneous output voltage is

$$v_o(t) = \sum_{n=1,3,5}^{\infty} B_n \sin n\omega t.$$

The coefficient B_n can be determined by considering a pair of pulses such that the positive pulse of duration δ starts at $\omega t = \alpha$ and the negative one of the same width starts at $\omega t = \pi + \alpha$.

The effects of all pulses can be combined together to obtain the effective output voltage.

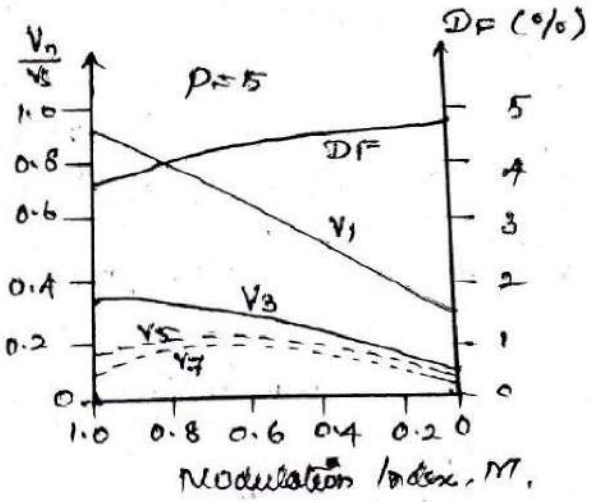
If the positive pulse of mth pair starts at $\omega t = \alpha_m$ and ends at $\omega t = \alpha_m + \delta$, the Fourier coefficient for a pair of pulses is

$$b_n = \frac{2}{\pi}\left[\int_{\alpha_m+\delta/2}^{\alpha_m+\delta} \sin n\omega t \, d(\omega t) - \int_{\pi+\alpha_m}^{\pi+\alpha_m+\delta/2} \sin n\omega t \, d(\omega t)\right]$$

$$= \frac{4V_s}{n\pi} \sin\frac{n\delta}{4}\left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right)\right]$$

The coefficient B_n can be found by adding the effects of all pulses.

$$B_n = \sum_{m=1}^{2p} \frac{4V_s}{n\pi} \sin\frac{n\delta}{4}\left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right)\right]$$



Harmonic profile of multiple-pulse width modulation

The switching time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = (m - M)\frac{T_s}{2} \quad \text{for } m = 1, 3, \ldots 2p.$$

$$t_m = \frac{\alpha_m}{\omega} = (m - 1 + M)\frac{T_s}{2} \quad \text{for } m = 2, 4, \ldots 2p.$$

Since all widths are same, pulse width d (or pulse angle δ) becomes,

$$d = \frac{\delta}{\omega} = t_{m+1} - t_m = mT_s .$$

where $T_s = T/2q$.

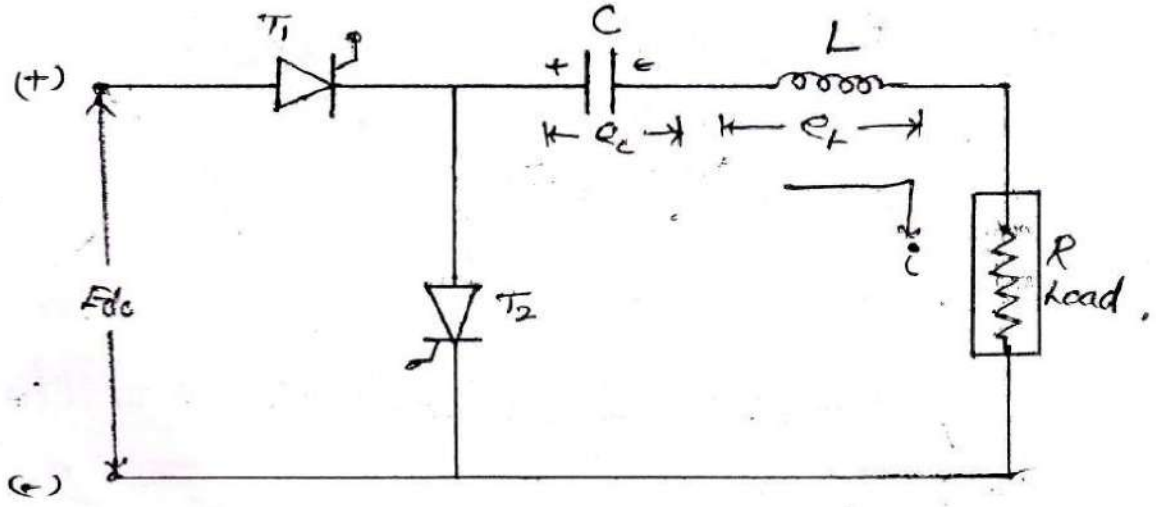
SERIES INVERTERS (SERIES RESONANT INVERTERS)

The commutating elements, L and C are connected in series with load is called Series Inverters. This constitute series RLC resonant circuit.

If the load is purely resistive, it only has resistance in the circuit.

In case of load being inductive or capacitive in nature, its Inductance or capacitance part is added to the commutating elements.

This type of thyristorised inverter produces an approximately sinusoidal waveform at a high output frequency ranging from 200 Hz to 100 KHz and is commonly used in relatively fixed output applications such as ultrasonic generators, induction heating, sonar transmitter, fluorescent lighting, etc. Due to the high - switching frequency, the size of commutating component is small.



Circuit Diagram.

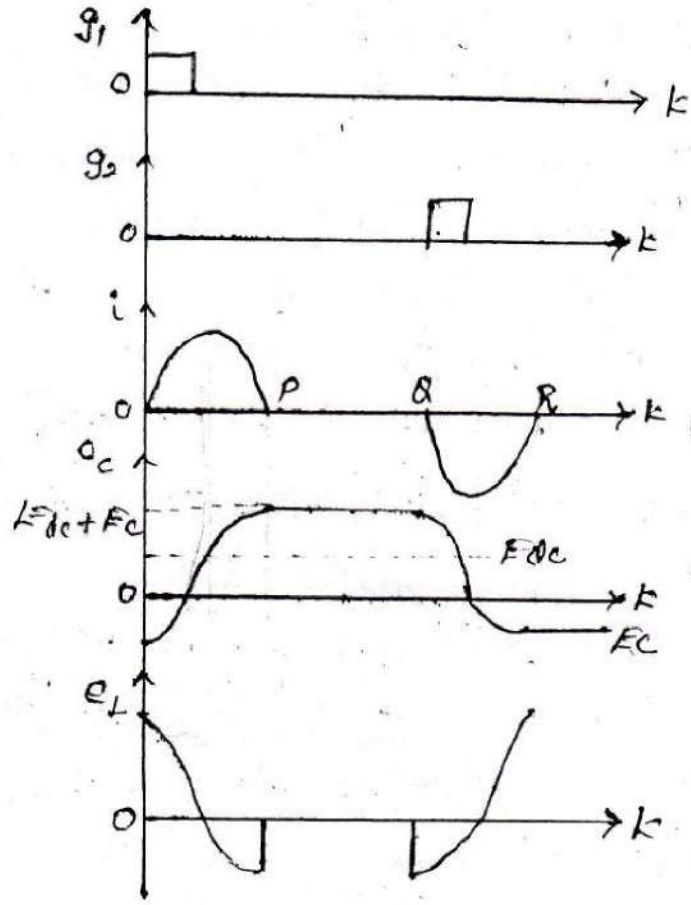
Two thyristors T_1 and T_2 are used to produce the two halves in the output.

The values of L and C are chosen such that, they form an underdamped circuit. This is necessary to produce the required oscillations.

This condition is fulfilled by selecting L and C such that

$$R^2 < \frac{4L}{C}$$

The operation of a basic series inverter circuit can be divided into following three operating modes.



Voltage and current waveforms

Mode : 1.

This mode begins when a d.c. voltage Edc is applied to the circuit and thyristor T_1 is triggered by giving external pulse to its gate.

As soon as T_1 is triggered, it starts conducting and resulting in some current to flow through the RLC series circuit.

Capacitor C gets charged up to voltage, say E_c with positive polarity on its left plate and negative polarity on its right plate. The load current is of alternating nature.

This is due to the underdamped circuit formed by the commutating elements.

It starts building up in the positive way, goes gradually to its peak-value, then starts returning and again becomes zero.

When the current reaches its peak-value, the voltage across the capacitor is approximately the supply voltage Edc. After this, the current starts decreasing but the capacitor voltage still increases and finally the current becomes zero but the capacitor retains the highest voltage (Edc + Ec), where Ec is the initial voltage across the capacitor at the instant SCR T_1 was turned-on. At P, SCR, is automatically turned-off because the current flowing through it becomes zero.

Mode : 2

During this mode, the load current remains at zero for a sufficient time (T_{off}). Therefore, both the

thyristors T_1 and T_2 are OFF. During this period PQ, capacitance voltage will be held constant.

Mode: 3.

Since the positive polarity of the capacitor C appears on the anode of SCR T_2, it is in conducting mode and hence triggers immediately.

At Q, SCR T_2 is triggered. When SCR T_2 starts conducting, capacitor C gets discharged through it.

Thus, the current through the load flows in the opposite direction forming the negative alternation. This current builds up to the negative maximum and then decreases to zero at point R.

SCR T_2 will then be turned-off. Now the capacitor voltage reverses to some value depending upon the values of R, L and C.

Again, after some time delay (T_{off}), SCR T_1 is triggered and in the same fashion other cycles are produced. This is a chain process giving rise to alternating output almost sinusoidal in nature.

The output frequency is given by

$$F = \left[\frac{1}{T/2 + T_{off}}\right] \text{Hz}.$$

Where T is the time period for oscillations and is given by

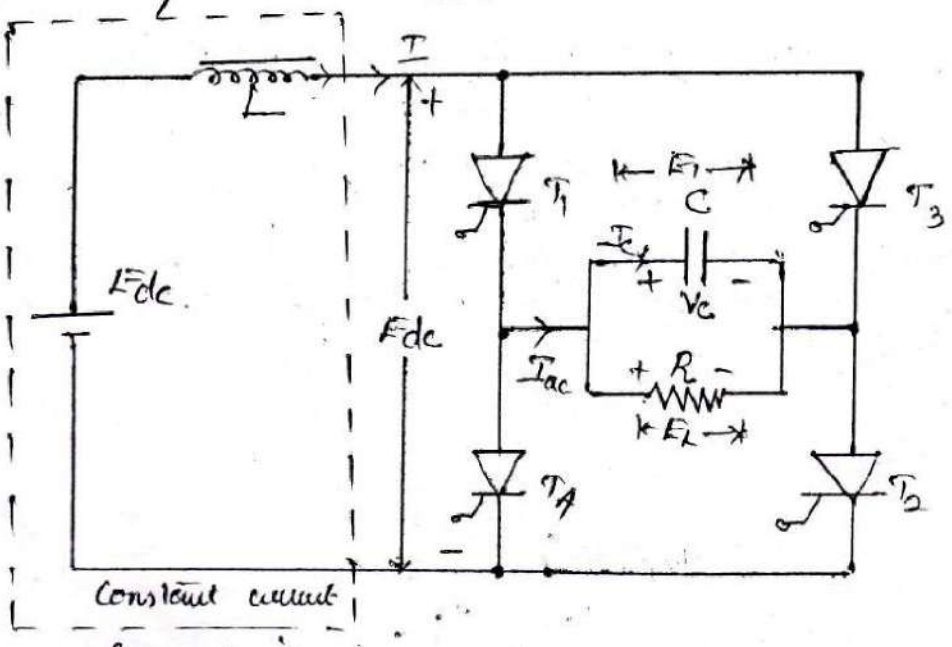
$$\frac{T}{2} = \frac{\pi}{\sqrt{1/LC - R^2/4L^2}}$$

CURRENT SOURCE INVERTERS.

In a current-source inverter (CSI), the current from the d.c. source is maintained at an effectively constant level, irrespective of load or inverter conditions. This is achieved by inserting a large inductance in series with the d.c. supply to enable changes of inverter voltage to be accommodated at low values of di/dt.

The d.c. input to current-source inverter is obtained from a fixed voltage a.c. source through a controlled rectifier bridge, or through a diode bridge and a chopper.

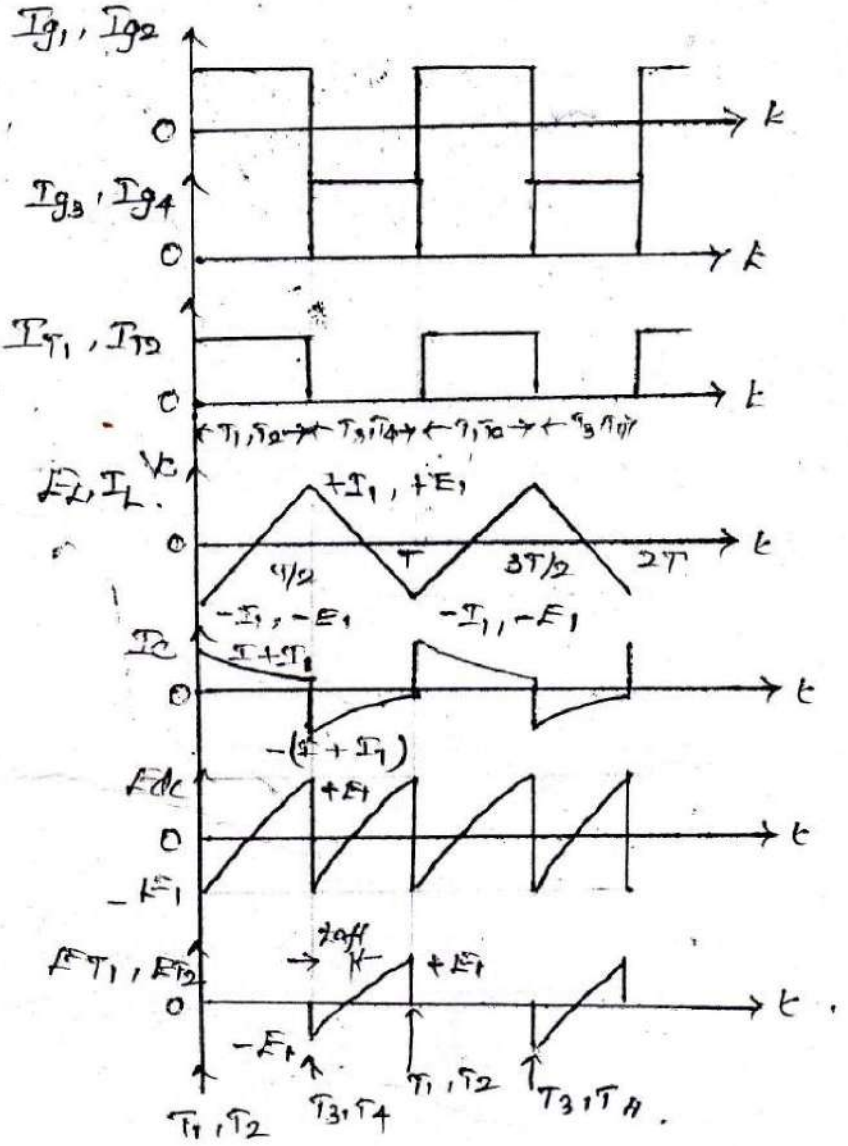
In order that current input to CSI is almost ripple free, L-filter is used before CSI. As it is a constant-current system, the current sourced inverter is used typically to supply high-power factor loads whose impedance either remains constant or decreases



Power diagram

that of V_c. When T_3, T_4 are gated at $t = T/2$, $V_c = E_1$ reverse-biases T_1, T_2. Hence turned-off immediately. The source current now flows through T_3, parallel combination of R, C and T_4.

From instant $\frac{T}{2}$ to T, $I_{T_3} = I_{T_4} = I$. but $I_{sc} = -I$. The variation of a.c current I_{ac} is a square of amplitude I_1.



Voltage and current waveforms

Applns: Speed ctrl of high power ac drives, Induction heating, Static VAR compensators, used as Power supplies in aircrafts (or) ship boards

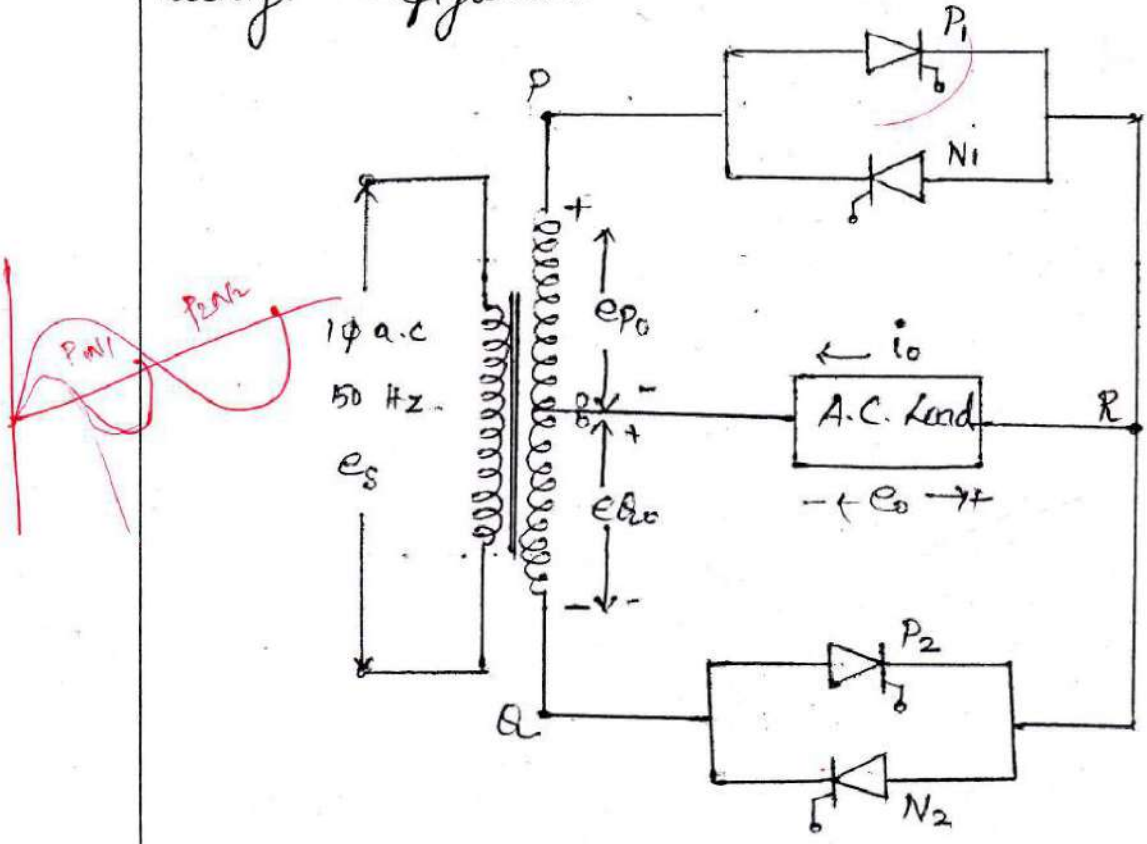
CYCLOCONVERTERS. (One stage freq changer)

A cycloconverter is a type of power controller in which an alternating voltage at supply frequency is converted directly to an alternating voltage at load frequency without any intermediate d.c. stage. types – Step down $f_o < f_s$ → supply freq
→ load freq
– Step up $f_o > f_s$

1φ to 1φ CYCLOCONVERTER.

In a single-phase cycloconverter whose input and output are single phase a.c. The input a.c voltage of supply frequency 50 Hz is converted into lower frequency a.c. output.

The are mainly two configurations for this type cycloconverter, viz centre-tapped transformer configuration and bridge configuration.



Single phase to Single phase cycloconverter circuit.

harmonic frequencies in order to prevent problems either on switching or with harmonic overvoltages.

Applications of Current Source inverters are

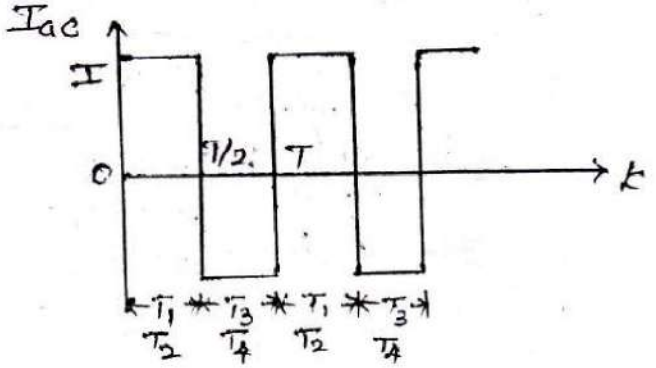
i) Speed control of a.c motors
ii) Induction heating
iii) Lagging VAR compensation
iv) Synchronous motor starting, etc.

Current source inverters may be either load commutated or force commutated. Load commutation is possible when load Pf is leading.

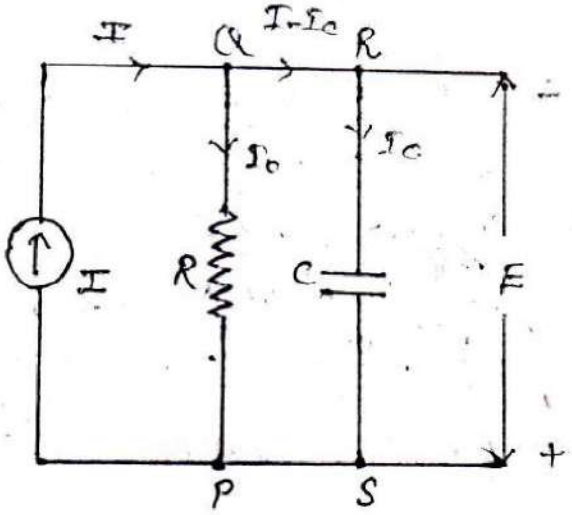
For lagging Pf loads, forced commutation is essential. Use of commutating capacitor is an important feature of force-commutated current-source inverters.

Single-Phase Capacitor-Commutated Current Source Inverters with Resistive Load.

Capacitor C in parallel with load is used for storing the charge for force commutating the SCRs. Thyristors T_1, T_2, T_3 and T_4 form the power bridge. These SCRs are triggered in pairs. T_1 T_2 together by gating signal I_{g1}, I_{g2} and T_3, T_4 by I_{g3}, I_{g4}.



a.c. Output current waveform.



Equivalent Circuit

Before $t=0$, let the capacitor voltage be $V_c = -E_1$ ie capacitor has right positive and left plate negative. At $t=0$, thyristor T_1 and T_2 are triggered, and when T_1 and T_2 become turned-on, capacitor applies reverse voltage across the previously conducting thyristors T_3, T_4 and hence turns them off.

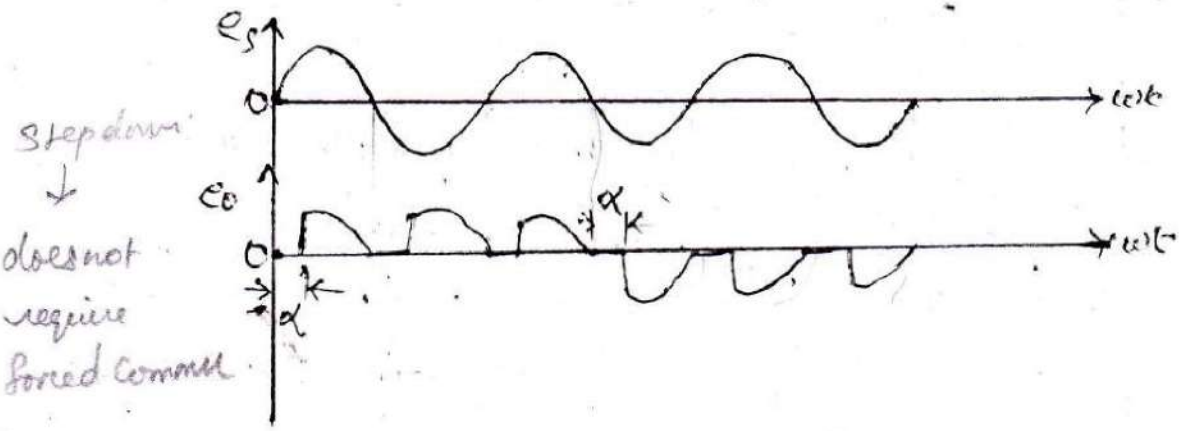
The source current I now flows through T_1, parallel combination of R and C and through T_2. From 0 to $T/2$, $I_{T1} = I_{T2} = I$, Output current $I_{dc} = I$, capacitor voltage V_c changes from $-E_1$ to $+E_1$ through the charging of C by current I_c.

Note that, here load voltage $E_L = V_c$. Thus the waveform of $I_L = E_L/R = V_c/R$ has the same nature as

(i) Centre-tapped Transformer Configuration

There are 4 thyristors, namely P_1, N_1, P_2 and N_2. Out of the four SCRs, SCRs P_1 and P_2 are responsible for generating the positive values forming the positive group. The other two SCRs N_1 and N_2, are responsible for producing the negative values forming the negative group.

This configuration is meant for generating 1/3 of the input frequency ie, this circuit generates a frequency of $16\frac{2}{3}$ Hz at its output.



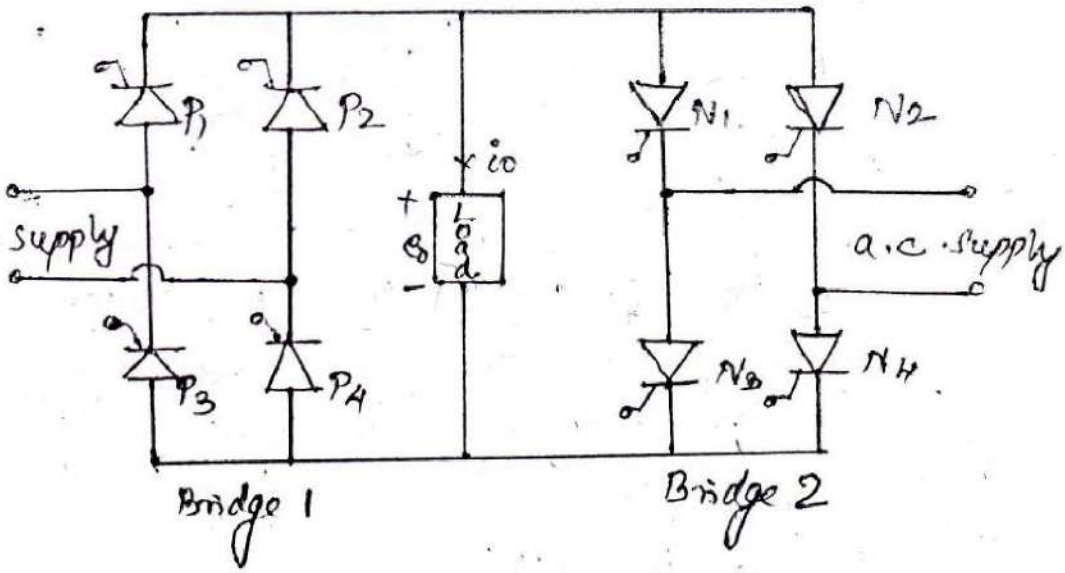
Step down
↓
does not require forced commutation

Input and output waveforms of a $16\frac{2}{3}$ Hz cycloconverter.

(ii) Bridge Configuration.

Two single phase fully-controlled bridges are connected in opposite directions.

Bridge 1 supplies load current in the positive half of the output cycle and bridge 2 supplies load current in the negative half of the output cycle. The two bridges should not conduct together as this will produce a short-circuit at the input.



Bridge configuration Single phase cycloconverter.

Instead of one thyristor in the centre-tap transformer configuration, two thyristors come in series with each voltage source in the bridge configuration.

For resistive loads, the SCRs undergo natural commutation and produce discontinuous current operation.

For inductive loads, the load current may be continuous or discontinuous, depending upon the firing angle and load power factor.

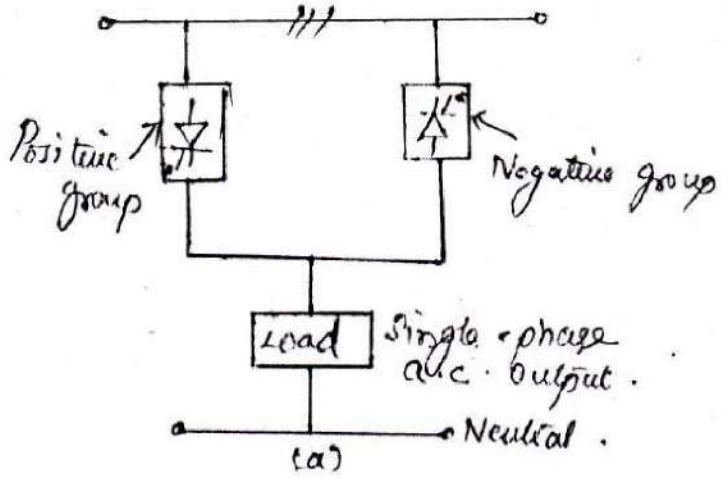
When the load current is positive, the firing pulses to the SCRs of bridge 2 will be inhibited and bridge 1 will be gated.

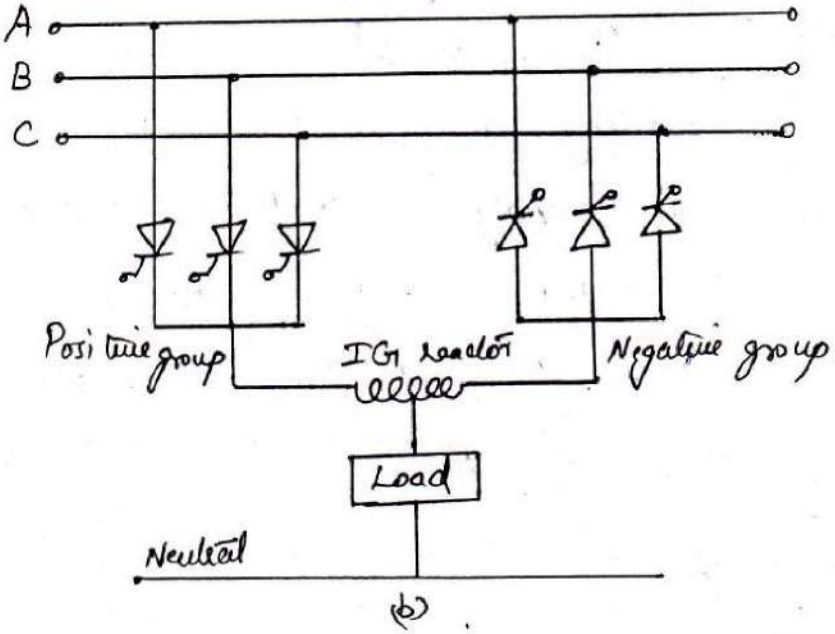
Similarly, when the load current is negative bridge 2 will be gated and the firing pulses will not be applied to the SCRs in bridge 1. This is the circulating current free mode of operation.

3φ to 1φ cycloconverters.

The type of three phase cycloconverter depends on the number of pulses used. The amount of ripple content can be reduced by increasing the number of pulses used.

In a thyristor converter circuit, current can only flow in one direction. For allowing the flow of current in both the direction during one complete cycle of load current, two three-phase half-wave converters must be connected in antiparallel.

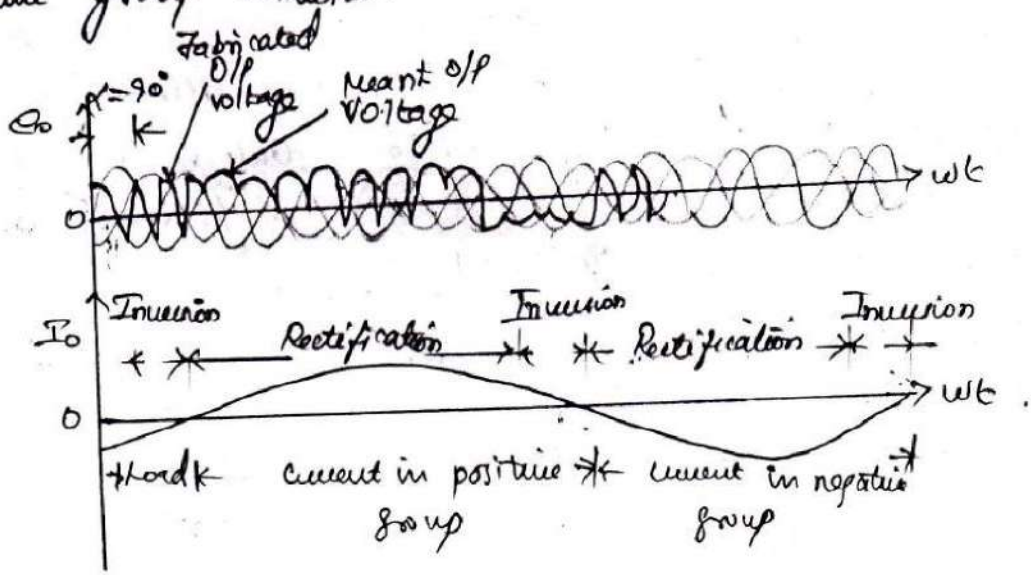




Three-phase to single-phase cycloconverter (a) schematic diagram (b) basic circuit configuration with IG reactor.

The converter circuit that permits the flow of current during positive half-cycle of low-frequency output current is called as positive-group converter.

The other group permitting the flow of current during the negative half cycle of output current is called as negative group converter.



Voltage and current waveform for a three-phase half-wave cycloconverter

A.C VOLTAGE REGULATORS.

By connecting a reverse parallel pair of thyristors or Triac between a.c supply and load, the voltage applied to the load can be controlled. This type of power controller is known as an a.c. voltage controller or a.c. regulators. Therefore a.c voltage regulators converts fixed mains voltage directly to variable alternating voltage without a change in the frequency.

Applications of A.C. Voltage controllers are

1. Speed control of polyphase induction motors,
2. Domestic and industrial heating.
3. Light control
4. On-load transformer tap changing,
5. Static reactive power compensators etc.

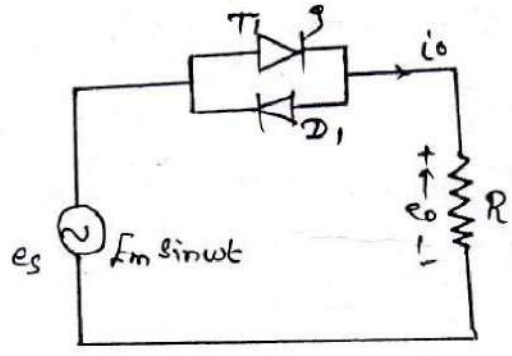
Classification of a.c. Voltage controllers

- Single-phase controllers
  - Unidirectional (or) Half-wave control
  - Bidirectional (or) Full-wave control.
- Three-Phase controllers.
  - Unidirectional (or) Half-wave control
  - Bidirectional (or) Full-wave control.

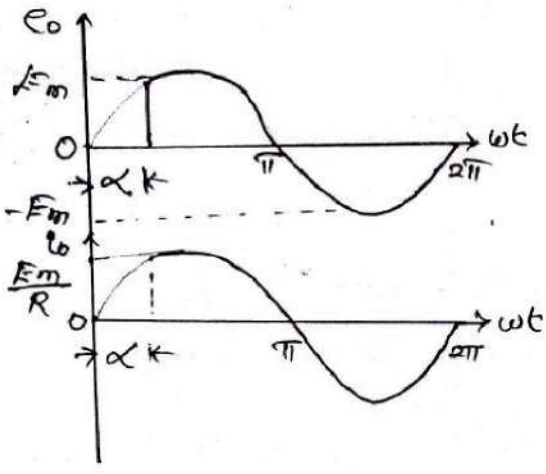
(i) Half-wave a.c. voltage regulators.

One thyristor is connected with one diode in antiparallel condition.

The power flow to the load is controlled by delaying the firing angle of thyristor T_1.



Power circuit



Voltage and current waveform.

The RMS output voltage is

$$E_0 = \left\{ \frac{1}{2\pi} \left[\int_{\alpha}^{\pi} 2E_s^2 \sin^2 \omega t \, d(\omega t) + \int_{\pi}^{2\pi} \alpha E_s^2 \sin^2 \omega t \, d(\omega t) \right] \right\}^{1/2}$$

$$= \left\{ \frac{2E_s^2}{4\pi} \left[\int_{\alpha}^{\pi} (1 - \cos 2\omega t) \, d(\omega t) + \int_{\pi}^{2\pi} (1 - \cos 2\omega t) \, d(\omega t) \right] \right\}^{1/2}$$

$$= E_s \left[\frac{1}{2\pi} \left(2\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2}$$

The average value of output voltage is given by

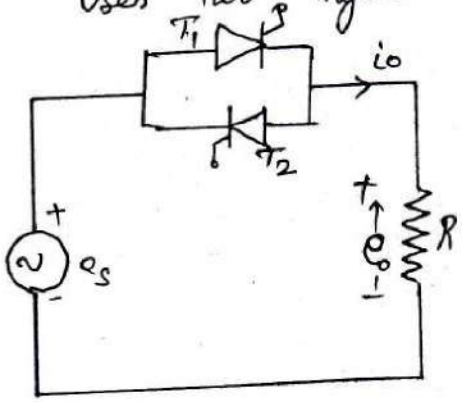
$$E_{oav} = \frac{1}{2\pi} \left[\int_{\alpha}^{\pi} \sqrt{2} E_s \sin \omega t \, d(\omega t) + \int_{\pi}^{2\pi} \sqrt{2} E_s \sin \omega t \, d(\omega t) \right]$$

$$= \frac{\sqrt{2} E_s}{2\pi} (\cos \alpha - 1)$$

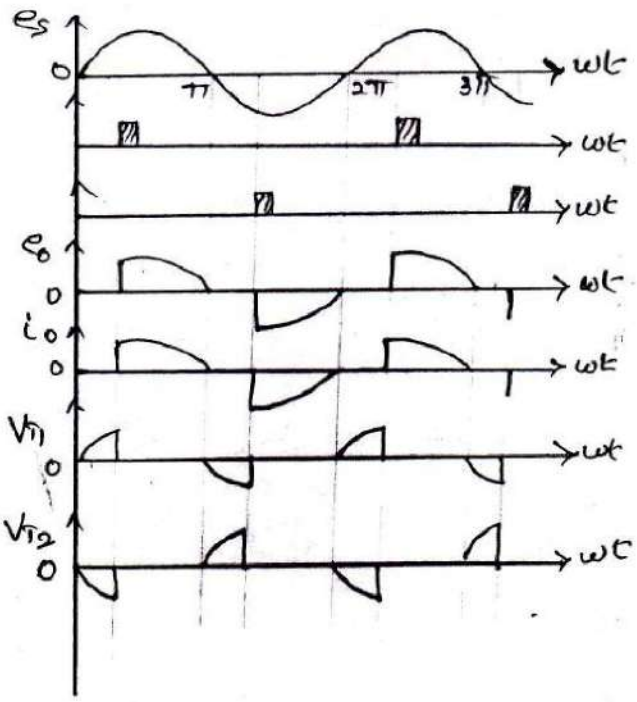
If α is varied from 0 to π, E_0 varies from E_s to $E_s/\sqrt{2}$ and E_{oav} varies from 0 to $\frac{-\sqrt{2} E_s}{\pi}$.

(ii) Fully-wave (Bidirectional) A.C. voltage controllers.

Uses two thyristors connected in antiparallel.



Single-phase a.c. voltage controller with R Load.



Voltage and Current Waveforms.

The Rms output voltage can be obtained from

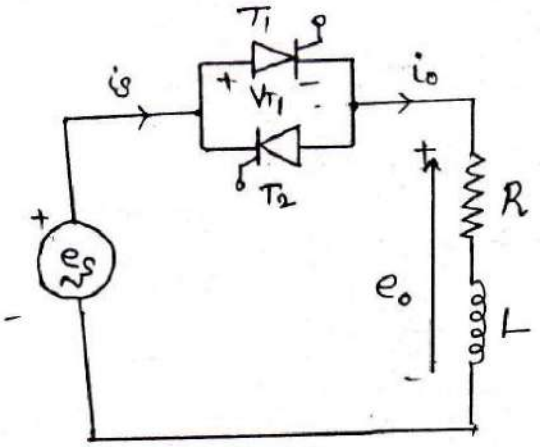
$$E_O = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi} 2E_s^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{4E_s^2}{4\pi}\int_{\alpha}^{\pi} (1-\cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

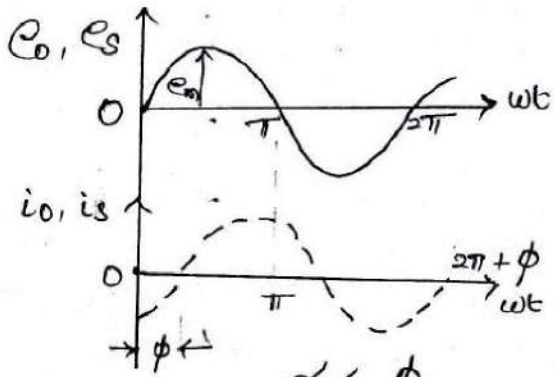
$$= E_s\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

Thus, by varying α from 0 to π, the Rms output voltage can be controlled from Rms input voltage E_s to zero.

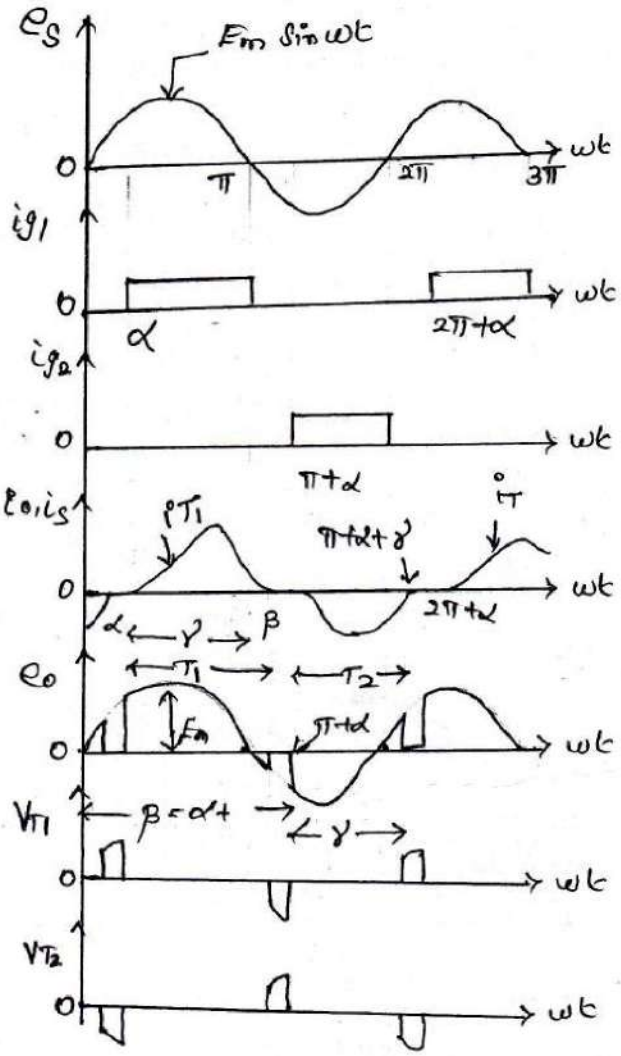
Single-phase a.c. voltage controller with inductive (RL)



Circuit diagram



$\alpha \leq \phi$



$\alpha > \phi$

The expression for load current is and β can be obtained as,

For $\alpha \leq \omega t \leq \beta$, the KVL is,

$$e_s = E_m \sin \omega t$$
$$= R.i_o + L.\frac{di_o}{dt}.$$

The solution of this equation is of the form,

$$i_o = \frac{E_m}{Z} \sin(\omega t - \phi) + A.e^{-(R/L)t}.$$

where

$$Z = (R^2 + \omega^2 L^2)^{1/2}$$

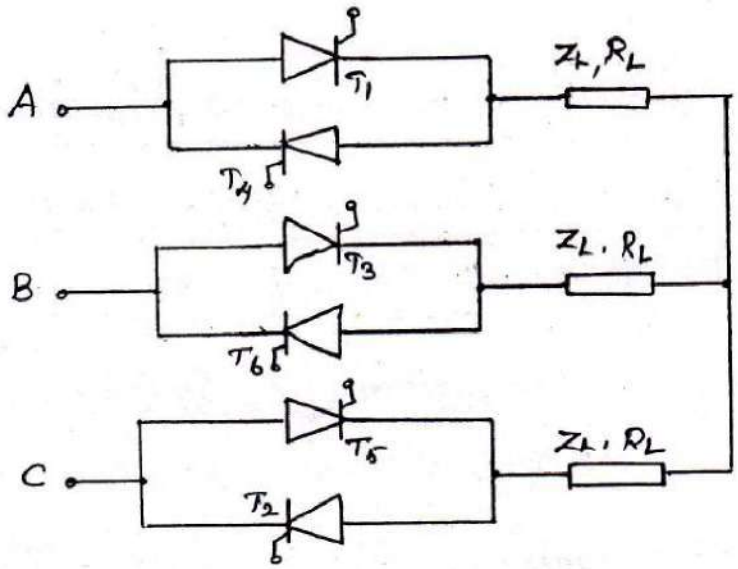
and

$$\phi = \tan^{-1} \frac{\omega L}{R}.$$

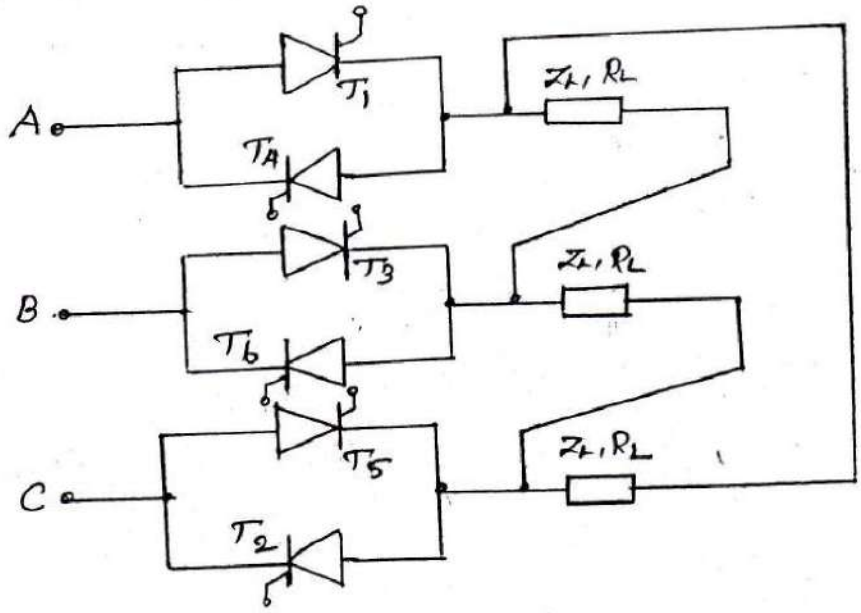
and.

$$\gamma = \beta - \alpha$$

Three - Phase A.C. Regulators.



3 - wire star load.



3-wire delta load.

Three-phase bidirectional Delta-Connected Regulators:

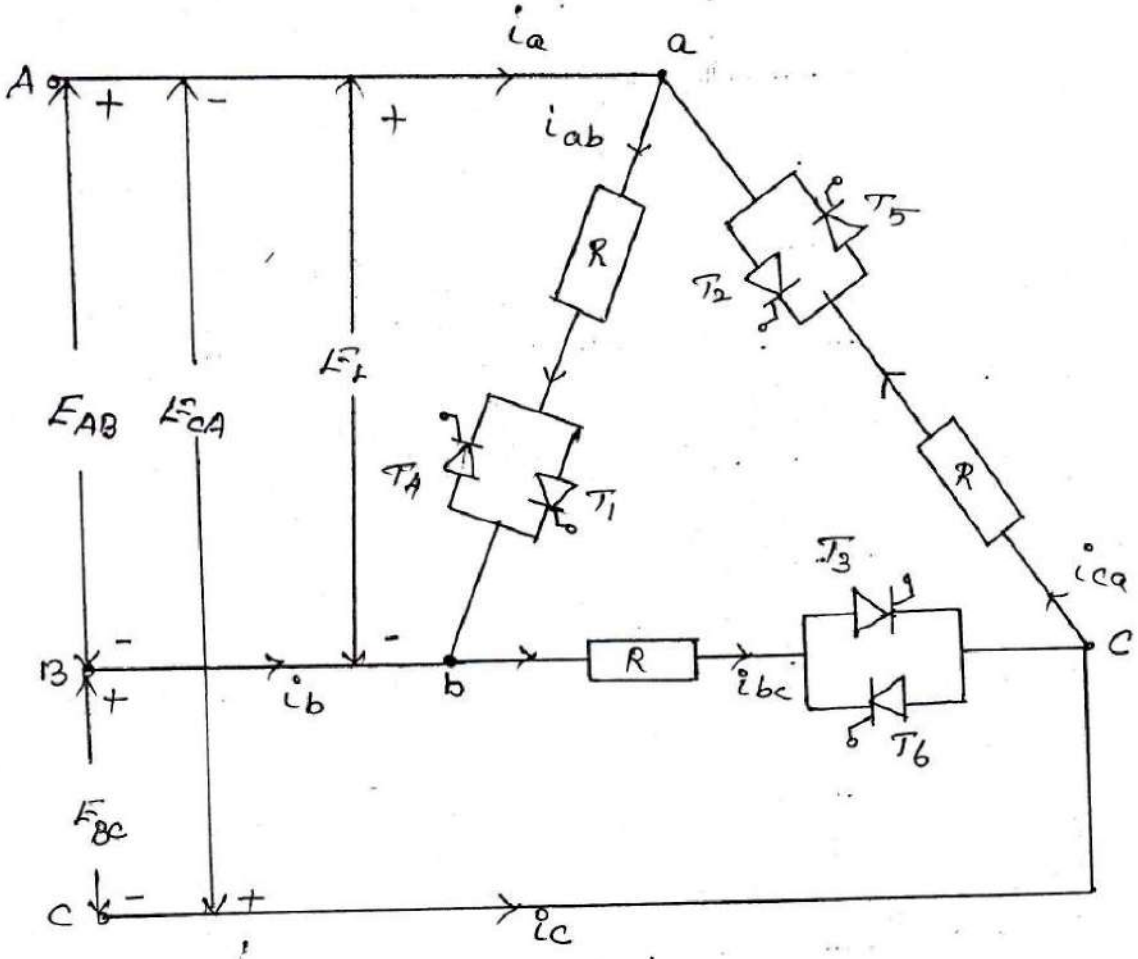
Since the phase current in a normal three-phase system is only $\frac{1}{\sqrt{3}}$ of the line current, the current ratings of thyristors would be less than that if thyristors were placed in the line.

The instantaneous line-to-line voltages are

$$E_{AB} = e_{ab} = \sqrt{2}\, E_s \sin \omega t.$$

$$E_{BC} = e_{bc} = \sqrt{2}\, E_s \cdot \sin(\omega t - 2\pi/3)$$

$$E_{CA} = e_{ca} = \sqrt{2}\, E_s \cdot \sin(\omega t - 4\pi/3)$$



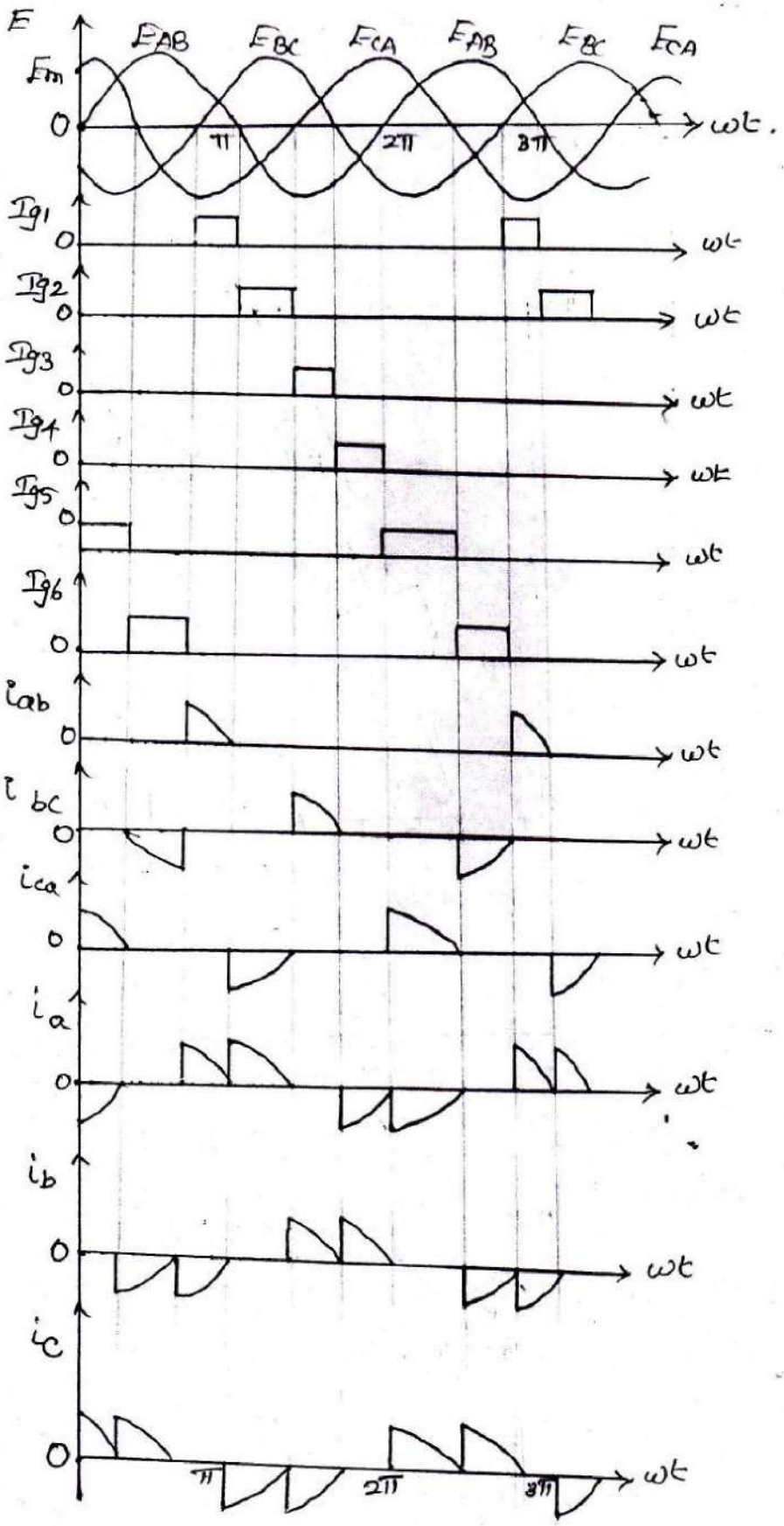
Delta connected three-phase a.c. regulator.

For $\alpha = 120°$, the input line voltages, phase and line currents, and thyristor gating signals are given below.

For resistive loads, the RMS output phase voltage can be obtained from

$$E_0 = \left[\frac{1}{2\pi}\int_{\alpha}^{2\pi} e_{ab}^2\, d(\omega t)\right]^{1/2} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi} 2E_s^2 \sin^2 \omega t\, d(\omega t)\right]^{1/2}$$

$$= E_s\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$



For $\alpha = 120°$.

Waveforms for three-phase delta-Connected regulator.

When $\alpha = 0$, the maximum output voltage would be obtained, and the control range of delay angle is

$$0 \leq \alpha \leq \pi.$$

The line current, which can be determined from the phase currents, are

$$i_a = i_{ab} - i_{ca}$$
$$i_b = i_{bc} - i_{ab}$$
$$i_c = i_{ca} - i_{bc}.$$

The RMS value of line and phase currents for the load circuit can be determined by numerical solution of (or) Fourier analysis.

If I_n is the rms value of the n^{th} harmonic component of a phase current, the RMS value of phase current can be obtained from

$$I_{ab} = \left[I_1^2 + I_3^2 + I_5^2 + I_7^2 + I_9^2 + I_{11}^2 + \cdots + I_n^2 \right]^{1/2}$$

Due to the delta connection, the triplen harmonic components (ie, those of order $n = 3m$, where m is an odd integer) of the phase currents would flow around the delta and would not appear in the line.

This is due to the fact that the zero sequence harmonics are in phase in all three phases of load.

The RMS line current becomes,

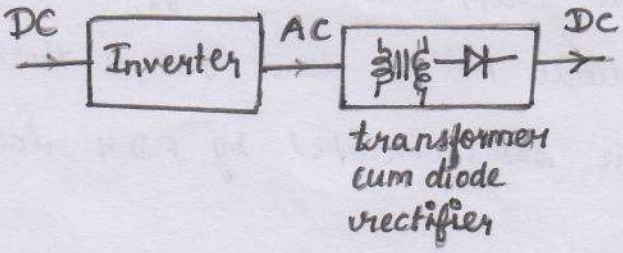
$$I_a = \left[\sqrt{3}\ I_1^2 + I_5^2 + I_7^2 + I_{11}^2 + \dots + I_n^2\right]^{1/2}$$

As a result, the RMS value of line current would not follow the normal relationship of a three phase system such that

$$I_a \angle \sqrt{3}\, I_{ab}.$$

Choppers - Introduction

AC Link chopper.

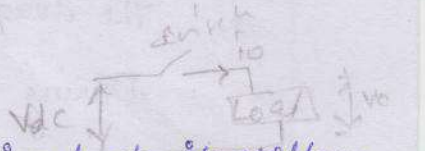


In the ac link chopper, dc is first converted to ac by an inverter (dc to ac converter).

AC is then stepped up or stepped-down by a transformer which is then converted back to dc by a diode rectifier.

As the conversion is in two stages, dc to ac & then ac to dc, ac link chopper is costly, bulky & less efficient.

DC Chopper

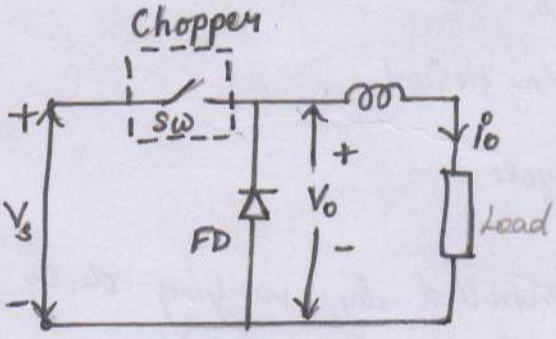


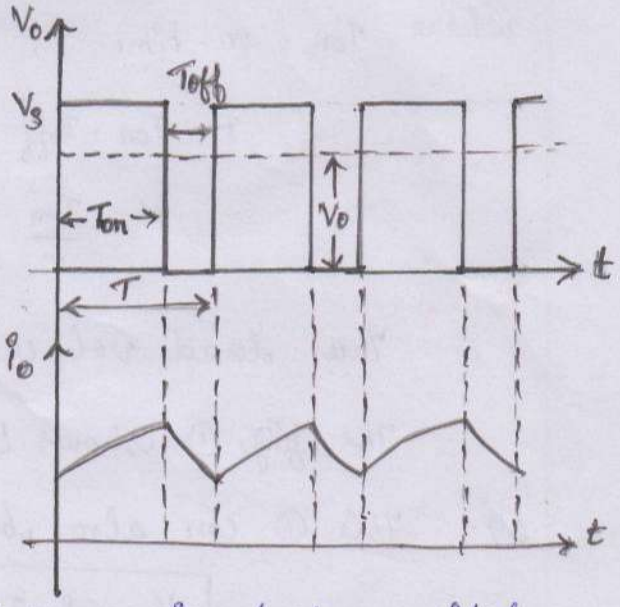
A chopper is a static device that converts fixed dc i/p voltage to a variable dc o/p vol directly.

Dc choppers are well used in trolley cars, marine hoists, forklift trucks & mine haulers, battery operated vehicles, traction motor control etc.

Adv: Greater efficiency, faster response, smooth ctrl, low maintenance, low cost

Step down Chopper.





Chopper is a high speed on/off semiconductor switch.

For the sake of highlighting the principle of chopper operation, the chopper is used for controlling the on, off periods of this switch is not shown.

During the period when chopper is on & load vol is equal to source vol V_s.

During the interval T_{off}, the chopper switches off, load current flows through the freewheeling diode FD. & load vol is therefore As a result, load terminals are short circuited by F.D & load voltage is therefore zero during T_{off}.

In this manner, a chopped dc vol is produced at the load terminals.

The load ckt as shown in fig is continuous.

During T_{on}, load ckt rises whereas during T_{off}, load ckt decays.

Avg load vol V_o is given by

$$V_o = \frac{T_{on}}{T_{on}+T_{off}} V_s$$

$$= \frac{T_{on}}{T} V_s \Rightarrow \boxed{V_o = \delta V_s} \longrightarrow (1)$$

where T_{on} = on-time ; T_{off} = off-time

$T = T_{on} + T_{off}$ = Chopping period.

$\alpha = \frac{T_{on}}{T}$ = duty cycle.

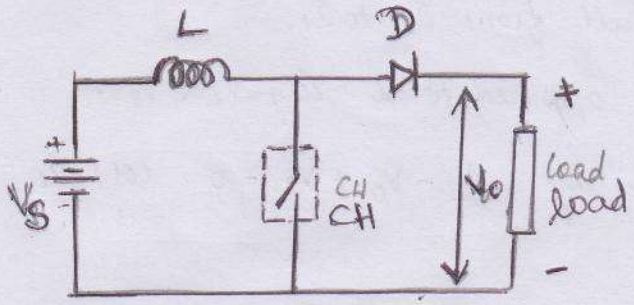
Thus load vol can be controlled by varying duty cycle α.

The eq (1) shows that the load vol is independent of load ckt. This (1) can also be written as

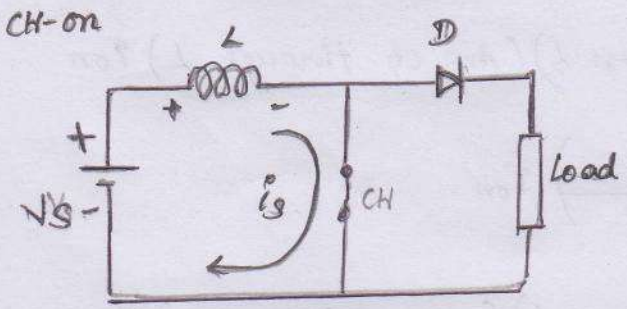
$$\boxed{V_o = f \cdot T_{on} \cdot V_s} \longrightarrow (2)$$

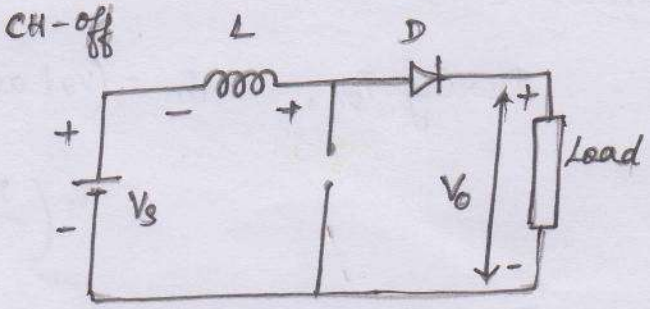
where ($\because f = \frac{1}{T}$ = Chopping freq)

Step-up Choppers



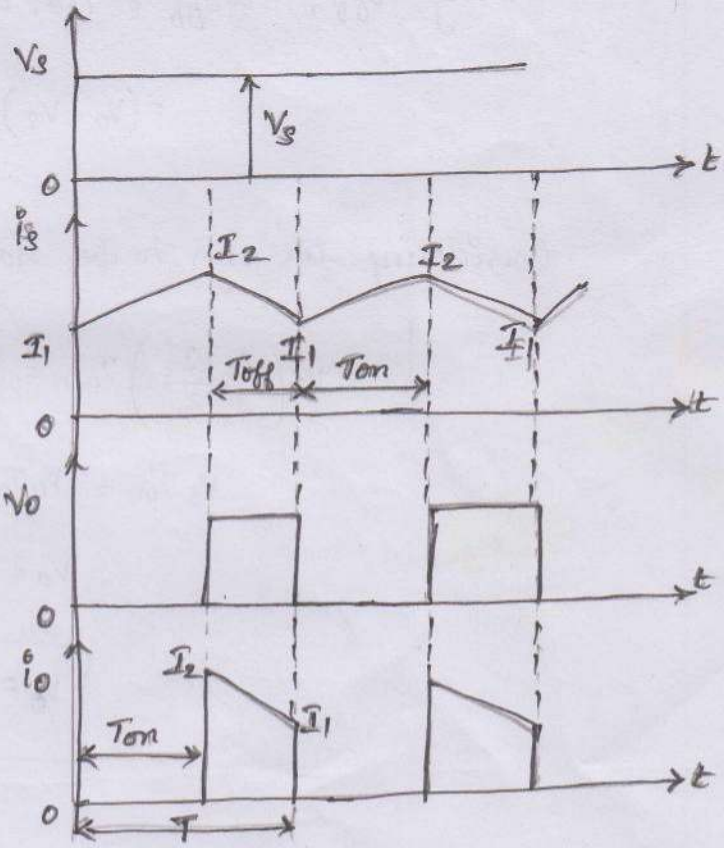
In step-up chopper, a large inductor L in series with source vol V_s is essential.





When the chopper CH is on, the closed current path is as shown in fig & the inductor stores energy during Ton period.

When CH is off, as the inductor cty cannot die down instantaneously, this cty is forced to flow through the diode & load for a time Toff.



As the cty tends to ↓, polarity of the emf induced in L is reversed.

As a result, vol across the load, given by $V_o = V_s + L\,(di/dt)$, exceeds the source vol V_s.

In this manner, the ckt acts as a step-up chopper & the energy stored in L is released to the load.

When CH is on, Ch through L would ↑ from I_1 to I_2.

When CH is off, Ch would fall from I_2 to I_1.

With CH-on, source vol is applied to L. ie, $V_L = V_s$.

When CH-off, KVL is given by $V_L - V_o + V_s = 0$ (or) $V_L = V_o - V_s$

Here $V_L \rightarrow$ vol across L.

During T_{on}, W_{in} = (vol across L)(Avg ch through L) T_{on}

$$= V_s \left(\frac{I_1 + I_2}{2} \right) T_{on}.$$

During T_{off}, W_{off} = (vol across L)(Avg ch through L) T_{off}

$$= (V_o - V_s) \left(\frac{I_1 + I_2}{2} \right) T_{off}.$$

Considering the sys to be lossless, $W_{in} = W_{off}$.

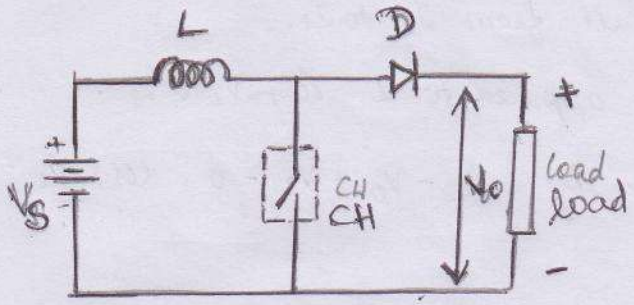
$$\therefore V_s \left(\frac{I_1 + I_2}{2} \right) T_{on} = (V_o - V_s) \left(\frac{I_1 + I_2}{2} \right) T_{off}$$

$$V_s T_{on} = V_o T_{off} - V_s T_{off}$$

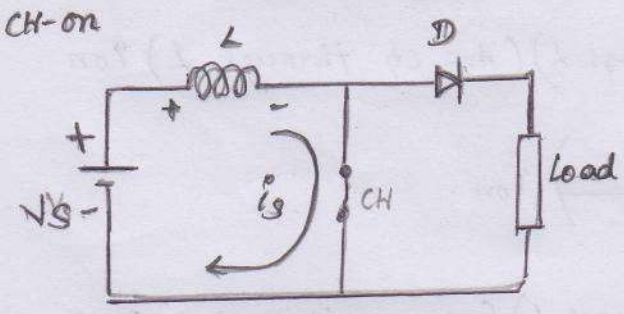
$$V_o = V_s \frac{T}{T_{off}} = V_s \left(\frac{T}{T - T_{on}} \right)$$

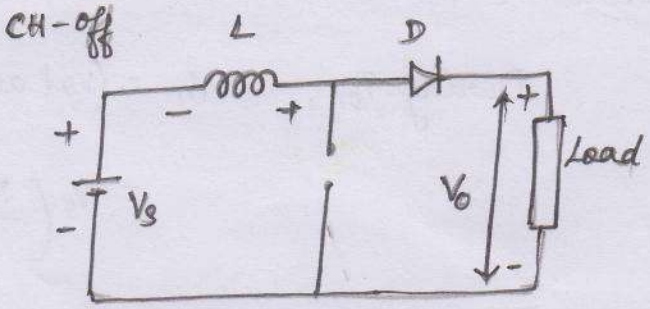
$$\boxed{V_o = V_s \left(\frac{1}{1-\alpha} \right)}$$

Step-up Choppers



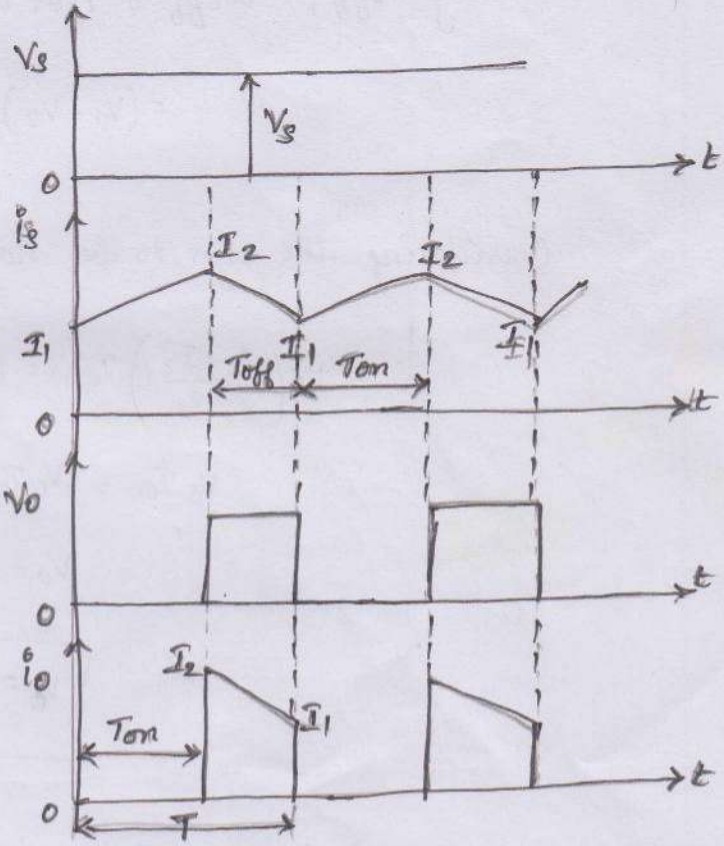
In step-up chopper, a large inductor L in series with source vol V_s is essential.





When the chopper CH is on, the closed current path is as shown in fig & the inductor stores energy during Ton period.

When CH is off, as the inductor cty cannot die down instantaneously, this cty is forced to flow through the diode & load for a time Toff.



As the cty tends to ↓, polarity of the emf induced in L is reversed.

As a result, vol across the load, given by $V_o = V_s + L\,(di/dt)$, exceeds the source vol V_s.

In this manner, the ckt acts as a step-up chopper & the energy stored in L is released to the load.

Control strategies of Chopper,

$V_o = V_{dc}\,\alpha$.

It is seen that, the avg value of o/p vol, V_o can be controlled by periadic opening & closing of the switches.

There are 2 types of ctrl strategies. 1) Time-ratio ctrl (TRC) & 2) Ct limit ctrl.

Time-Ratio ctrl (TRC)

In the time-ratio ctrl, the value of $\frac{T_{on}}{T}$ is varied.

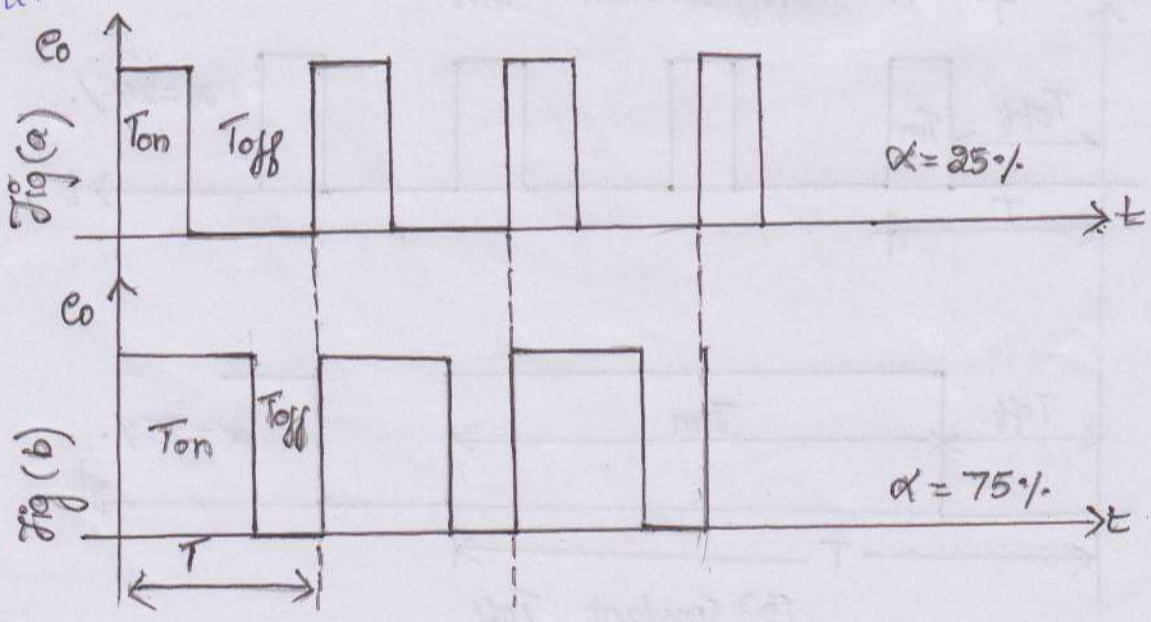
This is effected in 2 ways.

They are variable freq operation & const freq operation.

Const freq ctrl.

In this type of ctrl strategy, the on-time T_{on}, is varied but the chopping freq f ($f = 1/T$, & hence the chopping period T) is kept constant.

Variation of T_{on} means adjustment of pulse width, as such this control strategy is also called as pulse-width modulation ctrl.



The above fig illustrates the principle of pulse-width modulation.

As shown, chopping period T is constant

$T_{on} = \frac{1}{4} T$, so that duty cycle $\alpha = 25\%$ ⇒ from fig (a)

$T_{on} = \frac{3}{4} T$, so that duty cycle $\alpha = 75\%$.

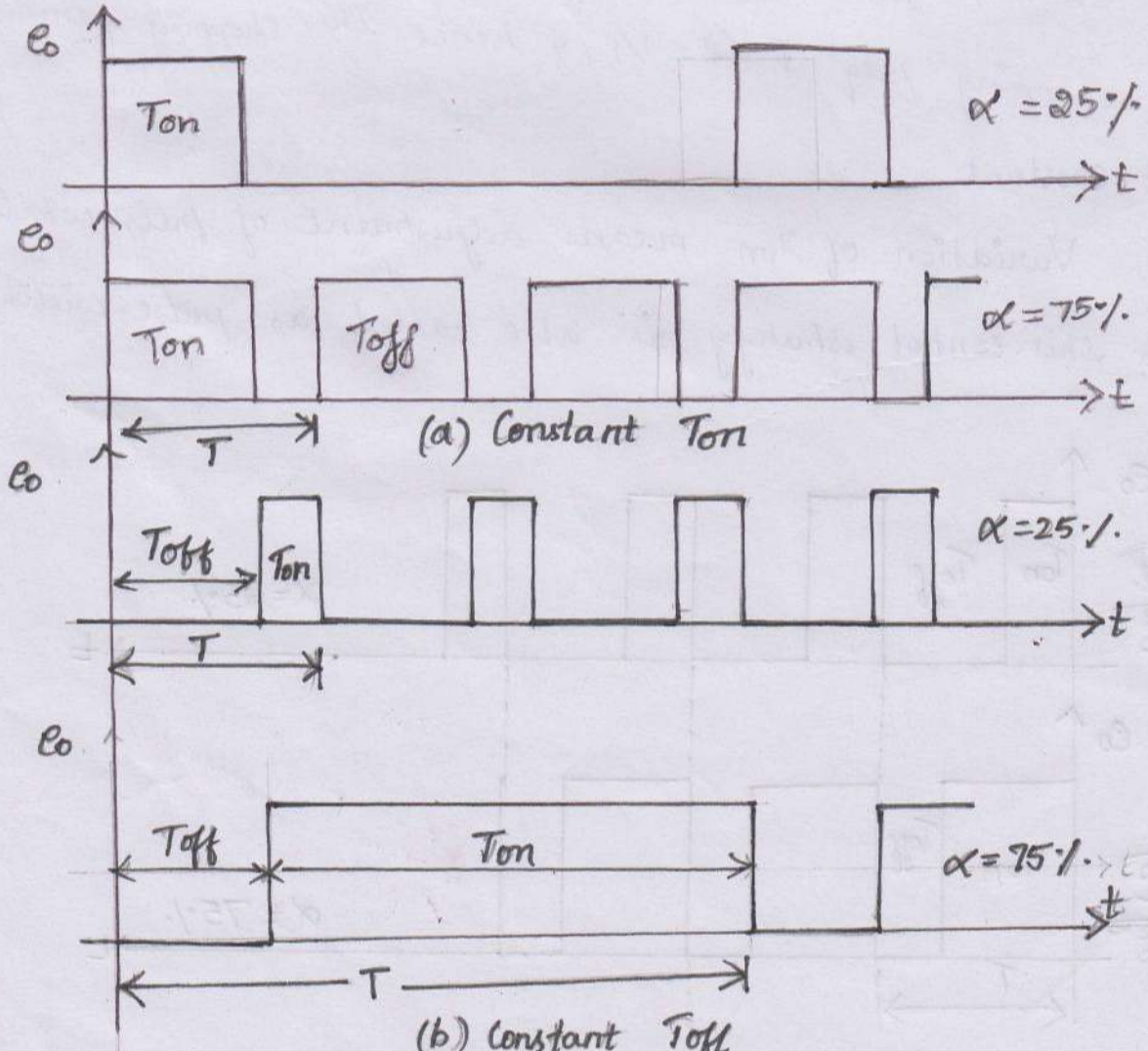
Hence, the o/p vol E_o can be varied by varying the on-time T_{on}.

Variable freq ctrl.

In this type of ctrl strategy, the chopping frequency f is varied & either

a) On-time T_{on}, is kept constant (or) b) Off time, T_{off} is kept const.

This type of ctrl strategy is also called as freq modulation ctrl.



As shown in fig (a) chopping period T is varied but on-time Ton is kept constant.

The o/p voltage waveforms are shown for two different duty cycles.

In fig (b), chopping period T is varied but Toff is kept constant.

Freq modulation control strategy has the following major disadvantages compared to PWM ctrl.

(i) The chopping freq has to be varied over a wide range for the ctrl of o/p vol in freq modulation. Filter design for such wide freq variation is, therefore, quite difficult.

(ii) For the ctrl of duty cycle, freq variation would be wide. As such, there is a possibility of interference with signalling & telephone lines in freq mody technique.

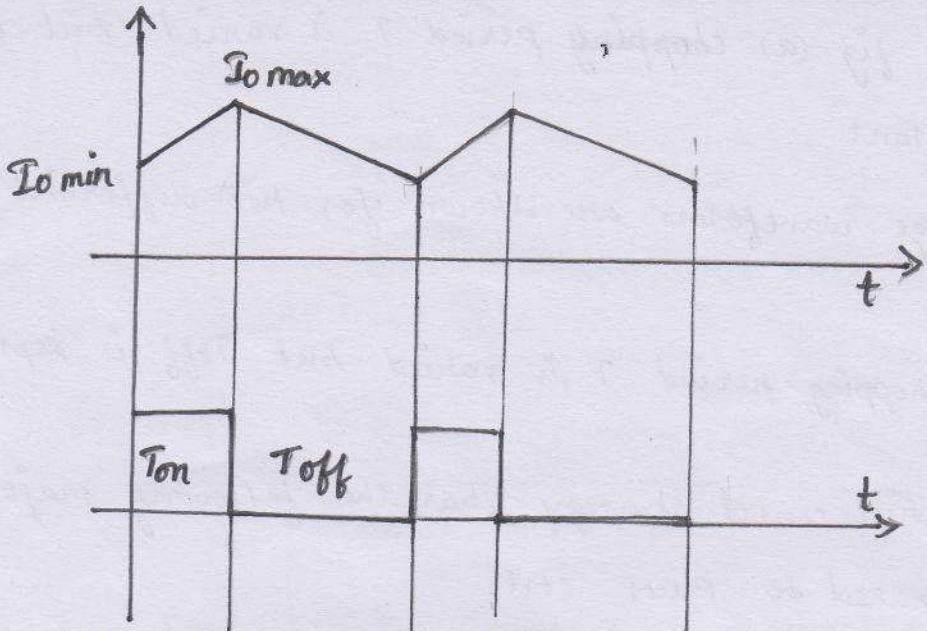
iii) The large off-time in freq mody technique may make the load ckt discontinuous, which is undesirable.

Thus, the constant freq sys (PWM) is preferred scheme for chopper drives.

Current limit control.

In current limit control strategy, the chopper is switched ON and OFF so that the current in the load is maintained b/w two limits.

When the current exceeds upper limit, the chopper is switched OFF. During OFF period, the load ckt freewheels & decreases exponential.



When it reaches the lower limit, the chopper is switch' on.

Ch limit ctrl is possible either with const freq or with costant Ton.

The current limit control is used only when the load has energy storage elements.

The reference values are the load current or load-voltage.

The above fig illustrates the principle of ch limit ctrl.

Since, the chopper operates blw prescribed ch limits, discontinuity cannot occur.

The difference blw Io max & Io min decides the switching frequency.

The ripple in the load ch can be reduced if the differen blw the Io max & Io min limits is min.

This in turn ↑s chopper frequency thereby ↑ing the switching losses.

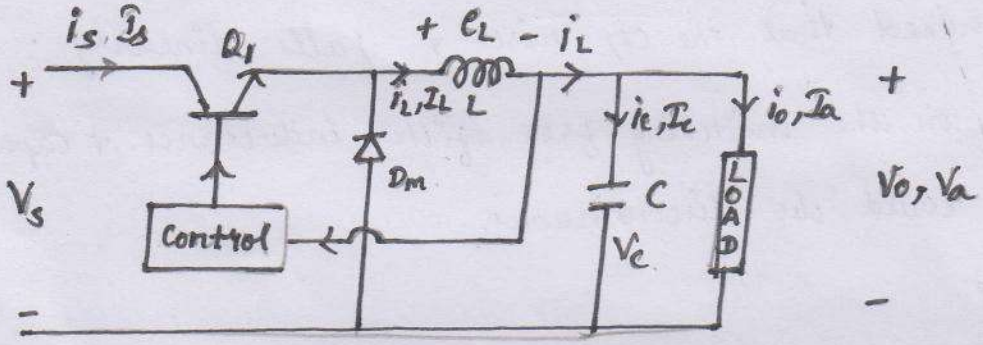
Switching mode regulators

DC Converters can be used as switching-mode regulators to convert a dc vol, normally unregulated, to a regulated dc o/p vol.

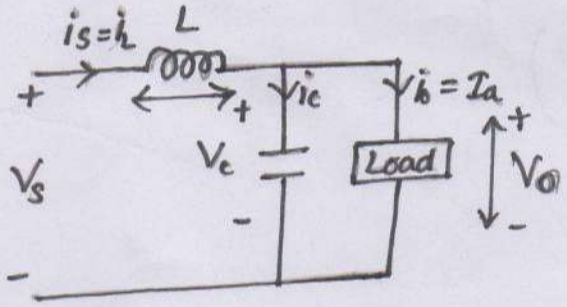
There are 4 basic topologies of switching regulators.

1) Buck regulators
2) Boost regulators
3) Buck-boost regulators
4) Cuk-regulators.

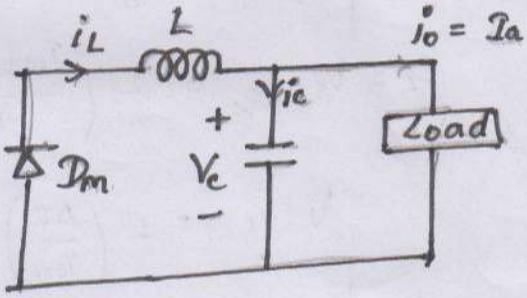
Buck regulators



Mode 1 : Q_1 on



Mode 2 : Q_1-off



In a buck regulator, the avg o/p vol V_a, is less than the i/p vol, V_s & hence the name "buck".

The ckt operation can be divided into two modes.

Mode 1 begins when Q_1 is switched on at $t = 0$.

The i/p ctt which rises, flows through filter inductor L, filter cap C, & load resis R.

Mode 2 begins when Q_1 is switched off at $t = t_1$.

The freewheeling diode D_m, conducts due to energy stored in the inductor; & the inductor c/t continues to flow through L, C, load & diode D_m.

The inductor c/t falls until Q_1 is switched on again in the next cycle.

The waveforms for the vol & c/t's are shown in fig for a continuous c/t flow in the inductor L.

It is assumed that the c/t rises & falls linearly.

Depending on the switching freq, filter inductance, & capacitance the inductor c/t could be discontinuous.

$$e_L = L \frac{di}{dt}$$

Voltage across L during ton period of the switch

$$e_L = V_s - V_o = L \left(\frac{I_{max} - I_{min}}{T_{on}} \right)$$

$$V_s - V_o = L \left(\frac{\Delta I}{T_{on}} \right)$$

$$T_{on} = L \left(\frac{\Delta I}{V_s - V_o} \right) \longrightarrow (1)$$

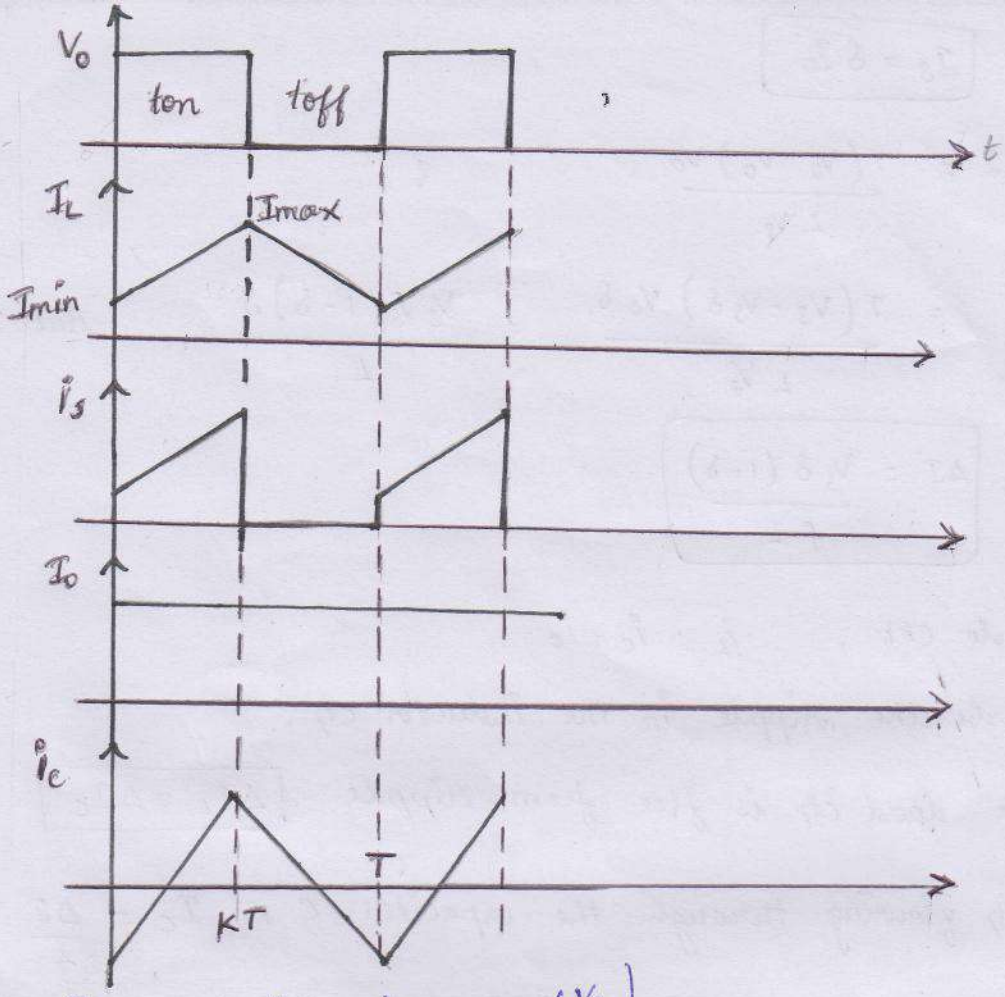
Voltage across L during T_{off}.

$$e_L = V_o = L \frac{\Delta I}{T_{off}}$$

$$T_{off} = L \left(\frac{\Delta I}{V_o} \right) \longrightarrow (2)$$

from (1) $\Rightarrow$ $\Delta I = \frac{t_{on} (V_s - V_o)}{L} \longrightarrow (3)$

from (2) $\Rightarrow$ $\Delta I = t_{off} \left(\frac{V_o}{L} \right) \longrightarrow (4)$



③ = ④ $\quad \frac{ton(V_s - V_o)}{L} = toff\left(\frac{V_o}{L}\right)$

$ton\,V_s - ton\,V_o = toff\,V_o$

$ton\,V_s = V_o\,(ton + toff)$

$V_o = \left(\frac{ton}{ton + toff}\right) V_s \Rightarrow \boxed{V_o = \delta V_s}$

Total time period $T = ton + toff$

Add ① & ②

$$T = L\left(\frac{\Delta I}{V_s - V_o}\right) + L\left(\frac{\Delta I}{V_o}\right)$$

$$T = L\Delta I\left(\frac{1}{V_s - V_o} + \frac{1}{V_o}\right)$$

$$\boxed{T = L\Delta I\left[\frac{V_s}{(V_s - V_o)V_o}\right]} \longrightarrow ⑤.$$

Assuming the sys to be loss less,

$V_s I_s = V_o I_o$.

$V_s I_s = V_s \delta I_o \quad (\because V_o = V_s \delta)$

$$I_s = \delta I_o$$

From (5) $\quad \Delta I = \dfrac{T(V_s - V_o)V_o}{L V_s}$

$$= \frac{T(V_s - V_s\delta)V_s\delta}{L V_s} = \frac{V_s T(1-\delta)\delta}{L} \qquad \text{But } T = \frac{1}{f}$$

$$\therefore \quad \boxed{\Delta I = \frac{V_s \delta (1-\delta)}{f L}}$$

Apply KCL to ckt, $\quad i_L = i_c + i_o$

Let δI_L be the ripple in the inductor ckt.

Assuming the load ckt is free from ripple $\quad \boxed{\Delta I_L = \Delta I_C}$

The Avg ckt flowing through the capacitor C, $\quad I_C = \dfrac{\Delta I}{4}$

The vol across the capacitor C

$$V_c = \frac{1}{C}\int_0^{T/2} I_c \, dt + V_c^o \quad (t=0)$$

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C}\int_0^{T/2} I_c \, dt.$$

$$\Delta V_c = \frac{1}{C}\,\frac{\Delta I}{4}\int_0^{T/2} dt$$

$$= \frac{1}{C}\,\frac{\Delta I}{4}\,[t]_0^{T/2}$$

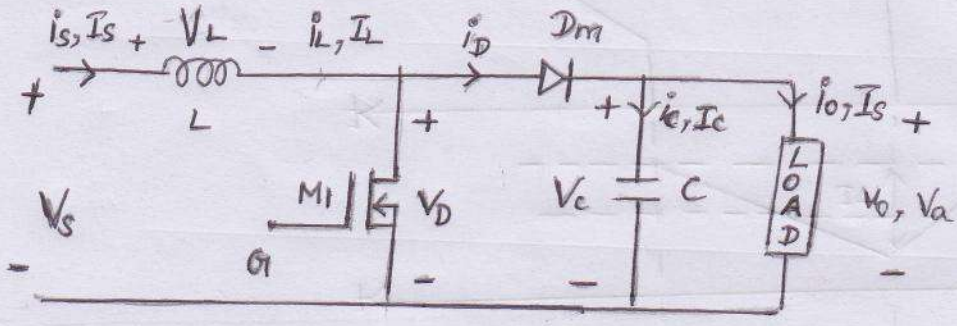
$$\Delta V_c = \frac{1}{C}\,\frac{\Delta I}{4}\left[T/2\right]$$

$$= \frac{\Delta I}{8C}\left(\frac{1}{f}\right)$$

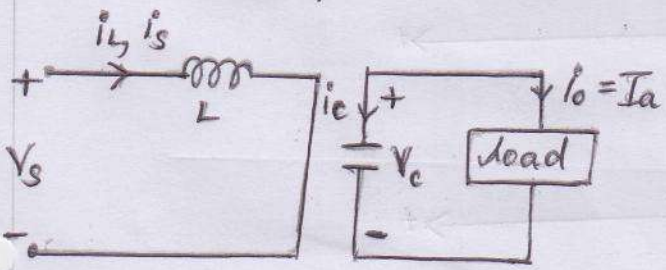
Sub ΔI $\quad \therefore \Delta V_c = \dfrac{1}{8Cf}\left[\dfrac{V_s \delta (1-\delta)}{f L}\right]$

$$\boxed{\Delta V_c = \frac{V_s \delta (1-\delta)}{8 C f^2 L}}$$

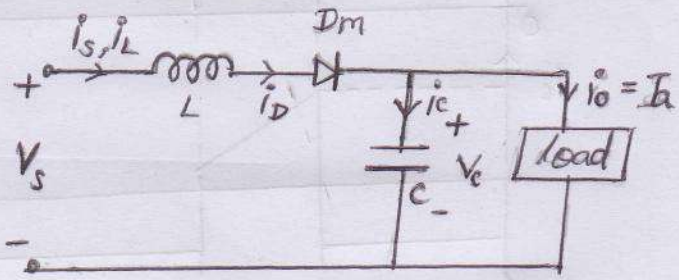
Boost regulators.



Mode 1



Mode 2



In boost regulator, the o/p vol is greater than the i/p vol- hence the name "boost".

The ckt operation can be divided into two modes.

Mode 1 begins when M_1 is switched on at $t = 0$.

The i/p ct, which rises, flows through L & Q_1.

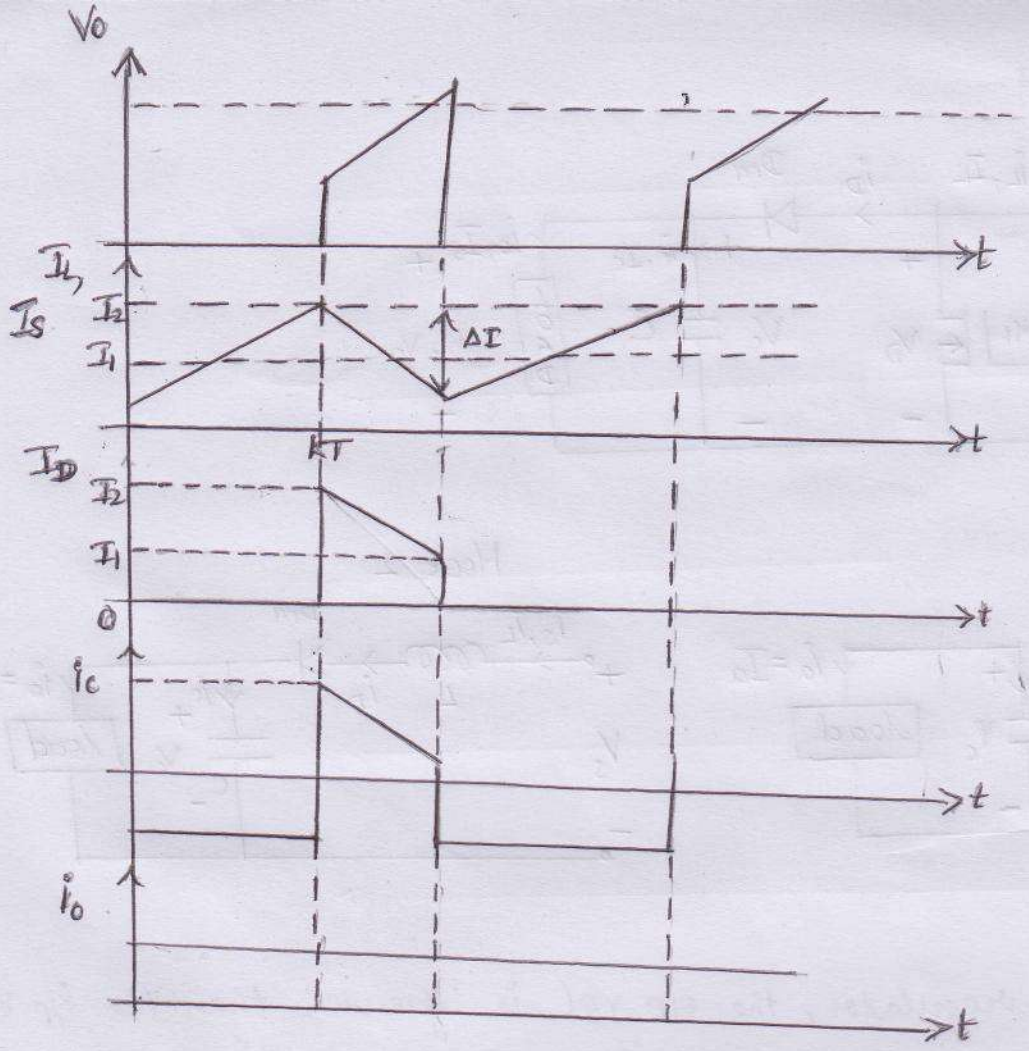
Mode 2 begins when M_1 is switched off at $t = t_1$.

The ct that was flowing through the transistor would now flow through L, C, load and diode D_m.

The L ct falls until M_1 is turned on again in the next cycle.

The energy stored in L is transferred to the load.

The waveforms for vol & cts are shown in fig for continuous load ct assuming that the ct rises or falls linearly.



Voltage across L $\quad V_L = L \frac{di}{dt}$

Vol across L during T_{on} of $T_1 \Rightarrow V_s = L\left(\frac{I_{max} - I_{min}}{T_{on}}\right)$

$$= L \frac{\Delta I}{T_{on}}.$$

$$\boxed{T_{on} = \frac{L \Delta I}{V_s}} \longrightarrow (1)$$

Vol across L during T_{off} of T_1

$$V_s - V_o = V_L = -L \frac{\Delta I}{T_{off}}.$$

$$T_{off} = \frac{-L \Delta I}{V_s - V_o} \longrightarrow (2).$$

From (1) $\quad \Delta I = \frac{T_{on} V_s}{L} \longrightarrow (3)$

From (2) $\quad \Delta I = -T_{off} \frac{(V_s - V_o)}{L} \longrightarrow (4)$.

④ = ② $T_{on}\frac{V_s}{L} = -\frac{T_{off}(V_s - V_o)}{L}$

$T_{on} V_s = -T_{off} V_s + T_{off} V_o$

$V_s(T_{on} + T_{off}) = V_o T_{off}$

$V_o = V_s\left(\frac{T_{on} + T_{off}}{T_{off}}\right) = V_s\left(\frac{T}{T_{off}}\right)$

$= V_s\left(\frac{T}{T - T_{on}}\right)$

$= V_s\left(\frac{1}{\frac{T}{T} - \frac{T_{on}}{T}}\right)$

$$\boxed{V_o = V_s\left(\frac{1}{1-\delta}\right)}$$

From ① & ②.

Total time period $T = T_{on} + T_{off}$

$T = L\left(\frac{\Delta I}{V_s}\right) + -L\left(\frac{\Delta I}{V_s - V_o}\right)$

$= L\Delta I\left(\frac{1}{V_s} - \frac{1}{V_s - V_o}\right)$

$= L\Delta I\left[\frac{V_s - V_o - V_s}{V_s(V_s - V_o)}\right] = L\Delta I\left(\frac{-V_o}{V_s(V_s - V_o)}\right)$

$T = \frac{1}{f} = \frac{L\Delta I V_o}{V_s(V_o - V_s)}$

Sub $V_o = \frac{V_s}{1-\delta}$ $\therefore T = \frac{L\Delta I\left(\frac{V_s}{1-\delta}\right)}{V_s\left[\left(\frac{V_s}{1-\delta}\right) - V_s\right]} = \frac{L\Delta I\left[\frac{V_s}{1-\delta}\right]}{V_s^2\left[\frac{1}{1-\delta} - 1\right]}$

$= \frac{L\Delta I}{(1-\delta)V_s\left[\frac{1-1+\delta}{1-\delta}\right]} = \frac{L\Delta I}{(1-\delta)V_s\left(\frac{\delta}{1-\delta}\right)}$

$$\therefore \quad T = \frac{1}{f} = \frac{L\,\Delta I}{V_s\,\delta}$$

$$\boxed{\Delta I = \frac{V_s\,\delta}{L\,f}}$$

Assuming the system to be loss less $\quad V_s I_s = V_o I_o$

$$V_s I_s = \left(\frac{V_s}{1-\delta}\right) I_o$$

$$\boxed{I_s = \frac{I_o}{1-\delta}}$$

Capacitor voltage

$$V_c = \frac{1}{C}\int_0^{ton} i_c\,dt + V_c(t=0)$$

$\hookrightarrow$ ∵ the capacitor is initially in charged condn.

$$V_c - V_c(t=0) = \frac{1}{C}\int_0^{ton} i_c\,dt$$

$$\Delta V_c = \frac{1}{C}\int_0^{ton} i_c\,dt$$

$$= \frac{1}{C}\int_0^{ton} I_o\,dt = \frac{I_o}{C}\left[t\right]_0^{ton}.$$

During Ton, capacitor is supplying I_o to load. ∴ $\boxed{i_o = i_c}$

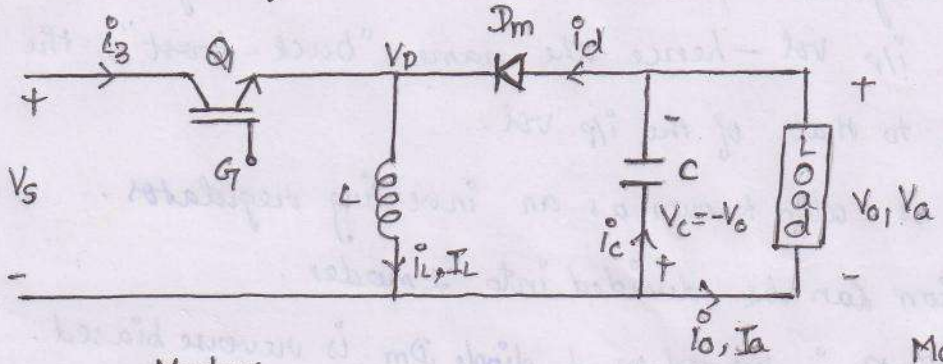
$$\Delta V_c = \frac{I_o}{C}\left[t\right]_0^{ton} = \frac{I_o}{C}\left[ton\right]$$

substitute ton $\Rightarrow \quad \Delta V_c = \frac{I_o}{C}\left[\frac{L\,\Delta I}{V_s}\right]$

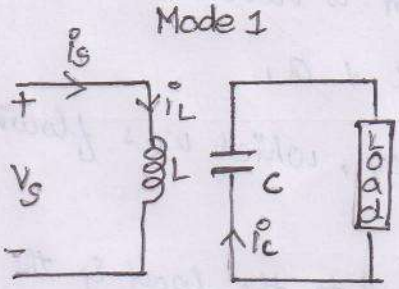
sub $\Delta I \Rightarrow \quad \Delta V_c = \frac{I_o}{C}\,\frac{L}{V_s}\left[\frac{V_s\,\delta}{L\,f}\right]$

$$\boxed{\Delta V_c = \frac{I_o\,\delta}{C\,f}}$$

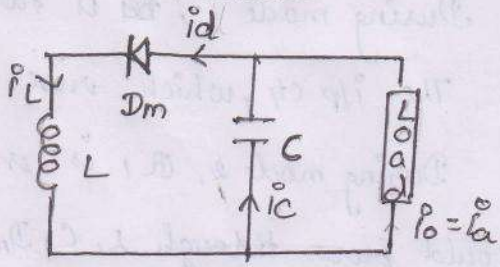
Buck - boost Regulators.

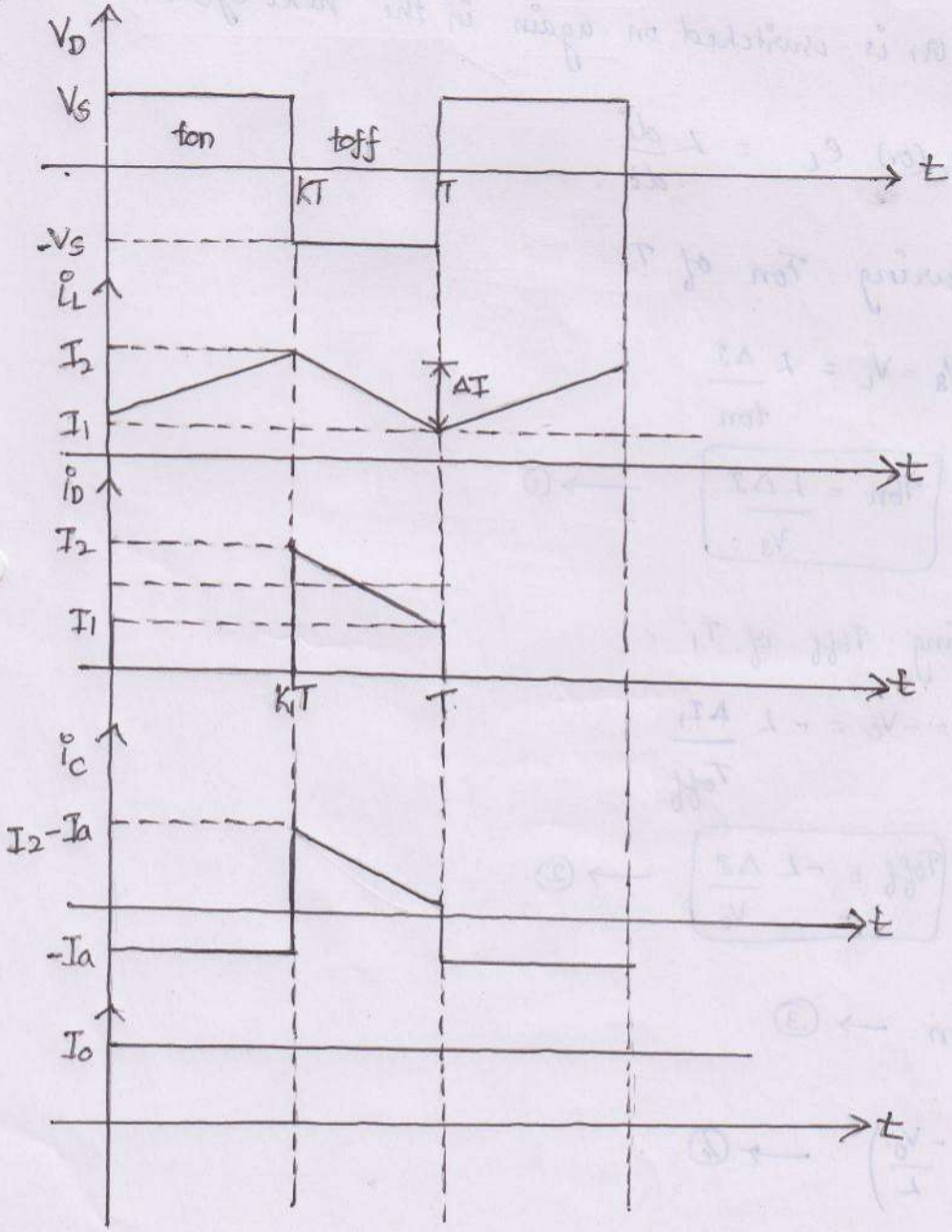


Mode 1



Mode 2





A buck-boost regulator provides an o/p vol that may be less than or greater than the i/p vol - hence the name "buck-boost"; the o/p vol polarity is opposite to that of the i/p vol.

This regulator is also known as an inverting regulator.

The ckt operation can be divided into 2 modes.

During mode 1, Q_1 is turned on & diode D_m is reverse biased.

The i/p ctr, which rises, flows through L & Q_1.

During mode 2, Q_1 is switched off & the ctr, which was flowing through L, would flow through L, C, D_m & the load.

The energy stored in L would be transferred to the load & the inductor ctr would fall until Q_1 is switched on again in the next cycle.

Vol across L $\quad V_L$ (or) $e_L = L \frac{di}{dt}$

Vol across L during Ton of T_1

$$V_s = V_L = L \frac{\Delta I}{t_{on}}$$

$$\boxed{T_{on} = \frac{L \Delta I}{V_s}} \longrightarrow (1)$$

Vol across L during Toff of T_1

$$V_o = -V_L = -L \frac{\Delta I_1}{T_{off}}$$

$$\boxed{T_{off} = -L \frac{\Delta I}{V_o}} \longrightarrow (2)$$

$(1) \Rightarrow \quad \Delta I = \frac{V_s}{L} t_{on} \longrightarrow (3)$

$(2) \Rightarrow \quad \Delta I = T_{off} \left(\frac{-V_o}{L} \right) \longrightarrow (4)$

③ = ④

$$\frac{V_s}{L} t_{on} = T_{off}\left(\frac{-V_o}{L}\right)$$

$$V_o = -V_s\left(\frac{T_{on}}{T_{off}}\right)$$

$$= -V_s\left(\frac{t_{on}}{T - t_{on}}\right)$$

$$= -V_s\left(\frac{1}{\frac{T}{t_{on}} - 1}\right) = -V_s\left(\frac{1}{\frac{1}{\delta} - 1}\right)$$

$$\boxed{V_o = -V_s\left(\frac{\delta}{1-\delta}\right)}$$

Total time period $T = T_{on} + T_{off}$.

$$= L\frac{\Delta I}{V_s} + \frac{-L\Delta I}{V_o}$$

$$= L\Delta I\left(\frac{1}{V_s} - \frac{1}{V_o}\right)$$

$$\frac{1}{f} = T = L\Delta I\left[\frac{V_o - V_s}{V_o V_s}\right]$$

put $V_o = \frac{-V_s\,\delta}{1-\delta}$

$$\therefore T = \frac{1}{f} = L\Delta I\left[\frac{\frac{-V_s\delta}{1-\delta} - V_s}{\left(\frac{-V_s\delta}{1-\delta}\right)V_s}\right]$$

$$= L\Delta I\left[\frac{-V_s\left[\left(\frac{\delta}{1-\delta}\right) + 1\right]}{\frac{-V_s^2\,\delta}{1-\delta}}\right]$$

$$= L\Delta I \left[\frac{1 + \frac{\delta}{1-\delta}}{\frac{V_s \delta}{1-\delta}} \right],$$

$$= L\Delta I \left[\frac{\frac{1-\delta+\delta}{1-\delta}}{\frac{V_s \delta}{1-\delta}} \right]$$

$$\boxed{T = L\Delta I \left[\frac{1}{V_s \delta} \right]}$$

Sub $T = \frac{1}{f} \Rightarrow \frac{1}{f} = L\Delta I \left(\frac{1}{V_s \delta} \right)$

$$\boxed{\Delta I = \frac{V_s \delta}{Lf}}$$

Assuming the system to be loss less

$$V_s I_s = -V_o I_o$$

$$V_s I_s = + \left[\frac{+V_s \delta}{1-\delta} \right] I_o .$$

$$\boxed{I_s = \left(\frac{\delta}{1-\delta} \right) I_o}$$

Capacitor voltage

$$V_c = \frac{1}{C} \int_0^{t_{on}} i_c \, dt + V_c(t=0)$$

$$V_c - V_c(t=0) = \frac{1}{C} \int_0^{t_{on}} i_c \, dt$$

$$\Delta V_c = \frac{I_c}{C} [t_{on}]$$

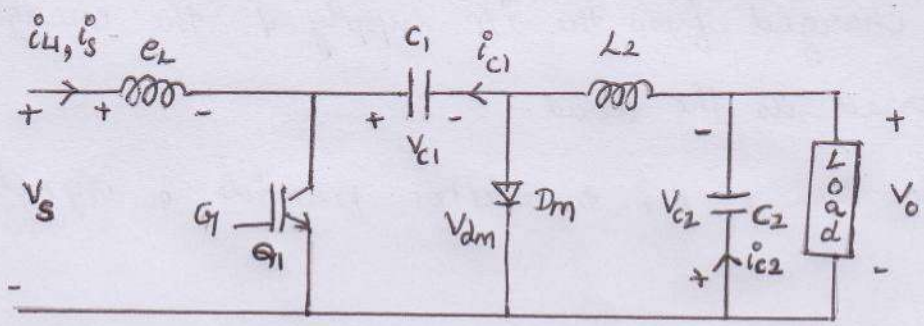
substitute t_{on} $\quad \Delta V_c = \frac{I_c}{C}\left[\frac{L\,\Delta I}{V_s}\right]$

sub ΔI $\quad \Delta V_c = \frac{I_c}{C}\left[\frac{1}{V_s}\left(\frac{V_s \delta}{L f}\right)\right]$

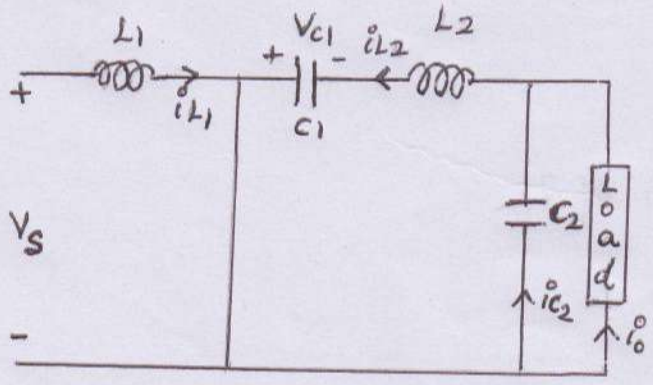
$$\Delta V_c = \frac{I_c}{C}\left(\frac{\delta}{f}\right) \qquad \text{Put } I_c = -I_o$$

$$\therefore \quad \boxed{\Delta V_c = -\frac{I_o \delta}{Cf}}$$

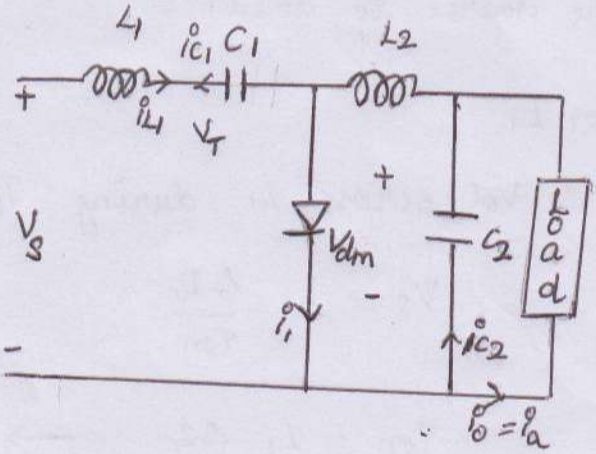
Cuk Regulator.



Mode 1 :



Mode 2 :



The ckt arrangement of the cuk regulator using a power BJT is shown in fig.

Unlike to the buck-boost regulator, the cuk regulator provides an o/p vol that is less than or greater than the i/p vol, but the o/p vol polarity is opposite to that of the i/p vol.

When the i/p vol is turned on & Q_1 is switched off, diode Dm is fwd biased & C_1 is charged through L_1, Dm, & the i/p supply V_s.

The ckt operation can be divided into 2 modes.

Mode 1 begins when Q_1 is turned on at $t = 0$.

The Ch through L_1 rises.

At the same time, the vol of C_1 reverse biases diode Dm turns it off.

The capacitor C_1 discharges its energy to the ckt formed by C_1, C_2, the load & L_2.

Mode 2 begins when Q_1 is turned off at $t = t_1$.

The C_1 is charged from the i/p supply & the energy stored in L_2 is transferred to the load.

The diode Dm & Q_1 transistor provide a synchronous switching action.

The capacitor C_1 is the medium for transferring energy from the source to load.

For L_1

Vol across L_1 during T_1 on of T_1

$$V_s = L_1 \frac{\Delta I_1}{T_{on}}.$$

$$T_{on} = L_1 \frac{\Delta I_1}{V_s} \longrightarrow (1)$$

During T_{off} Ch through L falls from I_{max1} to I_{min}, & voltage across L during T_{off} is $V_s - V_{c1}$

$$V_s - V_{c1} = -L_1 \frac{\Delta I_1}{T_{off}}$$

$$T_{off} = -\left(\frac{L_1 \Delta I_1}{V_s - V_{c1}}\right) \longrightarrow (2).$$

$$(1) \Rightarrow \Delta I_1 = \frac{T_{on} V_s}{L_1} \longrightarrow (a)$$

$$(2) \Rightarrow \Delta I_1 = \frac{T_{off}(V_{c1} - V_s)}{L_1} \longrightarrow (b)$$

$(a) = (b) \Rightarrow$ Avg voltage across capacitor C_1

$$\Delta I_1 = V_s t_{on} = (V_{c1} - V_s) t_{off}$$

$$V_s t_{on} = V_{c1} t_{off} - V_s t_{off}$$

$$V_s(t_{on} + t_{off}) = V_{c1} t_{off}$$

$$V_{c1} = V_s\left(\frac{T_{on} + T_{off}}{T_{off}}\right)$$

$$= V_s\left(\frac{T}{T - T_{on}}\right)$$

$$= V_s\left(\frac{1}{\frac{T}{T} - \frac{T_{on}}{T}}\right)$$

$$= V_s\left(\frac{1}{1 - \frac{T_{on}}{T}}\right)$$

$$\boxed{V_{c1} = V_s\left(\frac{1}{1-\delta}\right)} \longrightarrow (3).$$

During Ton of T_1, C/f through L_2 rises from I_{min2} to I_{max2}

i.e., $\Delta I_2 = I_{max2} - I_{min2}$.

Voltage across L_2 during on period of T_1

$$V_{C1} - V_{C2} = L_2 \frac{\Delta I_2}{t_{on}}.$$

Note. $-V_{C2} = V_o$

$$T_{on} = \frac{\Delta I_2 L_2}{V_{C1} + V_o} \rightarrow (4).$$

During Toff C/f through the L falls from I_{max2} to I_{min2}

$$V_o = -L_2 \frac{\Delta I_2}{T_{off}}$$

$$T_{off} = -\frac{L_2 \Delta I_2}{V_o} \rightarrow (5).$$

$$(4) \Rightarrow \Delta I_2 = \frac{T_{on}(V_{C1} + V_o)}{L_2}$$

$$(5) \Rightarrow \Delta I_2 = -\frac{T_{off} V_o}{L_2}$$

$$(4) = (5) \quad \frac{T_{on}(V_{C1} + V_o)}{L_2} = -\frac{T_{off} V_o}{L_2}$$

$$T_{on} V_{C1} + T_{on} V_o = -T_{off} V_o$$

$$V_o(T_{on} + T_{off}) = -T_{on} V_{C1}$$

$$V_{C1} = \frac{-V_o (T_{on} + T_{off})}{T_{on}}.$$

$$V_{C1} = -V_0\left(\frac{T}{T_{on}}\right),$$

$$= -V_0\left(\frac{1}{\frac{T_{on}}{T}}\right)$$

$$= -V_0/\delta$$

$$\therefore \boxed{V_{C1} = \frac{-V_0}{\delta}} \longrightarrow (6)$$

from (3) & (6)

$$V_s\left(\frac{1}{1-\delta}\right) = -\frac{V_0}{\delta}$$

$$\boxed{V_0 = \frac{-V_s\,\delta}{1-\delta}} \longrightarrow (7)$$

Considering the sys to be loss less

$$V_s I_s = -V_0 I_0.$$

sub V_0 $\quad V_s I_s = -\left(\frac{-V_s\delta}{1-\delta}\right) I_0$

$$\boxed{I_s = \frac{I_0\,\delta}{1-\delta}} \longrightarrow (8)$$

Total time period for L_1 $\quad T = t_{on} + t_{off}$

$$= \frac{L_1 \Delta I_1}{V_s} + \frac{-L_1 \Delta I_1}{V_s - V_{C1}}$$

$$= L_1 \Delta I_1 \left(\frac{1}{V_s} - \frac{1}{V_s - V_{C1}}\right)$$

$$= L_1 \Delta I_1 \left(\frac{V_s - V_{C1} - V_s}{V_s(V_s - V_{C1})}\right)$$

$$\frac{1}{f} = T = L_1 \Delta I_1 \left(\frac{-V_{C1}}{V_S (V_S - V_{C1})} \right)$$

$$\Rightarrow \Delta I_1 = \frac{-V_S (V_S - V_{C1})}{f V_{C1} L_1}$$

$$\Delta I_1 = \frac{V_S (V_{C1} - V_S)}{f V_{C1} L_1}$$

but $V_{C1} = \frac{V_S}{1-\delta}$ $\therefore$ sub V_{C1} $\Rightarrow$ $\Delta I_1 = \frac{V_S \left(\frac{V_S}{1-\delta} - V_S \right)}{f \left(\frac{V_S}{1-\delta} \right) L_1}$

$$\Delta I_1 = \frac{V_S \delta}{f L_1}$$

peak to peak ripple cf in L_1 $\Delta I_1 = \frac{V_S}{f L_1}$ $\rightarrow$ (10).

Total time for L_2 $T = T_{on} + T_{off}$

$$= \frac{\Delta I_2 L_2}{V_{C1} + V_O} - \frac{L_2 \Delta I_2}{V_O}$$

$$= L_2 \Delta I_2 \left[\frac{1}{V_{C1} + V_O} - \frac{1}{V_O} \right]$$

$$= L_2 \Delta I_2 \left[\frac{V_O - V_{C1} - V_O}{V_O (V_{C1} + V_O)} \right]$$

$$\frac{1}{f} = T = \frac{-L_2 \Delta I_2 V_{C1}}{V_O (V_{C1} + V_O)}$$ $\rightarrow$ (11).

peak to peak ripple ct in L_2

(11) $\Rightarrow$ $\Delta I_2 = \dfrac{-V_0(V_{C1}+V_0)}{L_2 V_{C1} f}$

Sub (3) & (4)

$$\Delta I_2 = \frac{-\left[\dfrac{V_s}{1-\delta} + \left(\dfrac{-V_s\delta}{1-\delta}\right)\right]\left[\dfrac{-V_s\delta}{1-\delta}\right]}{L_2\left[\dfrac{V_s}{1-\delta}\right] f}$$

$$= \frac{-1}{L_2 f}\left[\frac{\left(\dfrac{V_s}{1-\delta} - \dfrac{V_s\delta}{1-\delta}\right)\left(\dfrac{-V_s\delta}{1-\delta}\right)}{\dfrac{V_s}{1-\delta}}\right]$$

$$= \frac{-1}{L_2 f}\left[\frac{\left(\dfrac{-V_s\delta}{1-\delta}\right) V_s\left(\dfrac{1-\delta}{1-\delta}\right)}{\dfrac{V_s}{1-\delta}}\right]$$

$$= \frac{-1}{L_2 f}\left[-V_s\delta\right]$$

$$\boxed{\Delta I_2 = \frac{V_s\delta}{L_2 f}} \longrightarrow (12)$$

When T_1 is off, C_1 is charged by i/p ct for $T = T_{off}$.

Avg charging ct $I_C = I_s$

peak to peak ripple voltage of C_1

$$\Delta V_{C1} = \frac{1}{C_1}\int_0^{T_{off}} I_C\, dt = \frac{1}{C_1}\int_0^{T_{off}} I_s\, dt = \frac{I}{C_1}\left[T_{off}\right]$$

Sub (2) $\quad \therefore \Delta V_{C1} = \frac{I_S}{C_1}\left[\frac{-L_1 \Delta I_1}{V_S - V_{C1}}\right]$

sub the value of V_{C1} (3).

$$\Delta V_{C1} = \frac{-I_S L_1 \Delta I_1}{C_1\left[V_S - \frac{V_S}{1-\delta}\right]} = \frac{-I_S L_1 \Delta I_1}{C_1 V_S\left[\frac{1-\delta-1}{1-\delta}\right]} = \frac{-I_S L_1 \Delta I_1}{-C_1 V_S\left(\frac{\delta}{1-\delta}\right)}$$

sub ΔI_1 (10)

$$\Delta V_{C1} = \frac{I_S L_1 (1-\delta)}{C_1 V_S \delta}\left[\frac{V_S \delta}{L_1 f}\right]$$

$$\boxed{\Delta V_{C1} = \frac{I_S (1-\delta)}{C_1 f}} \longrightarrow (13)$$

If we assume that load ripple ch^{n}. so I_0 is negligible.

$$\therefore \Delta I_{L2} = \Delta I_{C2} + \cancel{I_0}^{0} \Rightarrow \boxed{\Delta I_{L_2} = \Delta I_{C_2}}$$

Average charging ch^{n} of capacitor C_2 which flows for time $T/2$ becomes $\quad I_{C_2} = \frac{\Delta I_2}{4}$

Peak to peak ripple voltage across C_2

$$\Delta V_{C2} = \frac{1}{C_2}\int_0^{T/2} I_{C_2}\, dt = \frac{1}{C_2}\int_0^{T/2} \frac{\Delta I_2}{4}\, dt = \frac{\Delta I_2}{4C_2}\left[\frac{T}{2}\right]$$

$$= \frac{\Delta I_2}{8C_2}\left[\frac{1}{f}\right]$$

But $\Delta I_2 = \frac{V_S \delta}{L_2 f} \quad \therefore \Delta V_{C2} = \frac{1}{8 f C_2}\left(\frac{V_S \delta}{L_2 f}\right)$

$$\boxed{\Delta V_{C2} = \frac{V_S \delta}{8 f^2 L_2 C_2}} \longrightarrow (14).$$