LECTURE NOTES

ON

Basic Electronics

1st and 2nd SEMESTER

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UNIT-I

Chapter-1: Semiconductor Diodes.

Introduction:

Semiconductor is a chemical Element in which the conductivity lies between conductor and insulator, Hence the movement of electrons (Current Conduction) can be controlled easily by means of an external voltage (Biasing).

Two types of Semiconductors
1. Intrinsic Semiconductor (Pure Semiconductor) and
2. Extrinsic Semiconductor (Impure semiconductor/Added impurity)

Extrinsic semiconductor is further classified into two types
a. P-Type Extrinsic Semiconductor (Doping Trivalent element) and
b. N-Type Extrinsic Semiconductor (Doping Pentavalent element).

The holes are majority charge carriers and electrons are minority charge carriers in P-Type and electrons are majority and holes are minority charge carriers in case of N-Type Semiconductor.

P-N Junction(Semiconductor Diode/ Diode):

***Construction:* +**

Starting with a piece of intrinsic semiconductor and divide it into two halves, one half is doped with any tri-valent element such as Boron, Aluminum etc., to form P-Type semiconductor, in which the holes are majority charge carriers and electrons are minority charge carriers. Other half is doped with any penta-valent element such as phosphorus, arsenic etc., to form N-Type Semiconductor, in which the electrons are majority charge carriers and holes are minority charge carriers.

The Junction or a line dividing the P-Type and N-Type is called P-N Junction. Metallic contact is connected to P-Type and N-Type material to get terminals for the device called Electrodes such as Anode and Cathode, this device is called P-N Junction Diode or Semiconductor diode or simply Diode as shown in figure(1).

Figure(1): P-N Junction Diode/Diode

Working:

The working principle can be studied in three different operations or Biasing arrangements as follows.

Case (1): Zero Biasing.

Without any external supply and at normal room temperature, at the time of contact with P-Type and N-Type material, it has a tendency to move or diffusing the electrons from N side and

occupies holes from the P side. Similarly holes in the P side attract electrons in the N side. This results forming a thin layer near the P-N Junction due to loosing electrons near the junction from the N side and holes near the junction from the P side. This layer or region is called depletion layer and it acts as an intrinsic semiconductor as shown in figure (2).

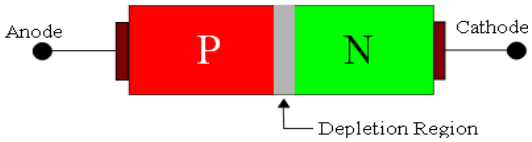


Figure (2): P-N Junction Diode/Diode with depletion layer/region.

Case (2): Reverse Biasing.

External supply with Positive terminal of the battery is connected to the cathode and negative terminal of the battery is connected to the anode is called Reverse biasing.

With this biasing the negative terminal of the battery sucks out or attracts the holes from P- Type material and positive terminal of the battery sucks out or attract electrons from N-Type material, this results wider depletion region and the resistance is very high, and the current that flows through the device only due to minority charge carriers as shown in figure (3).

The magnitude of current under reverse biasing is in terms of nano amperes for silicon diodes.

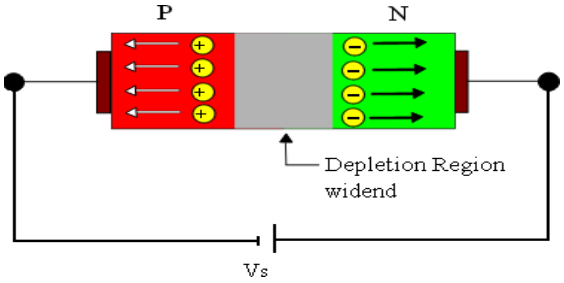


Figure (3): P-N Junction Diode is under Reverse Biasing.

Case (3): Forward Biasing.

External Supply with Positive terminal of the battery is connected to the anode and negative terminal of the battery is connected to the cathode is called forward biasing.

With this biasing the negative terminal of the battery pushes or pumps more electrons to the N-Type material and positive terminal of the battery pushes or pumps more holes to the P-Type material. By go on increasing the biasing voltage the width of the depletion region decreases, Resistance decreases and the current flowing through the device is increases(not proportional to voltage). If the Biasing voltage V_S is greater than or equal to V_γ (Thresold Voltage) the depletion layer completely vanishes and easily current will flow as shown in figure (4).The cut in voltage or threshold voltage (V_γ) for silicon diodes is 0.7 V and for Germanium diodes is 0.3V.

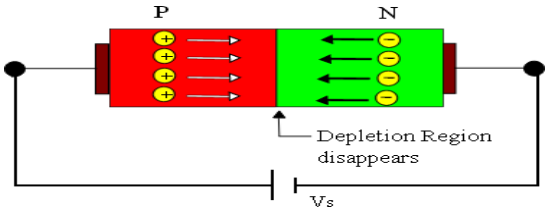


Figure (4): P-N Junction Diode is under Forward Biasing.

V-I Characteristics:

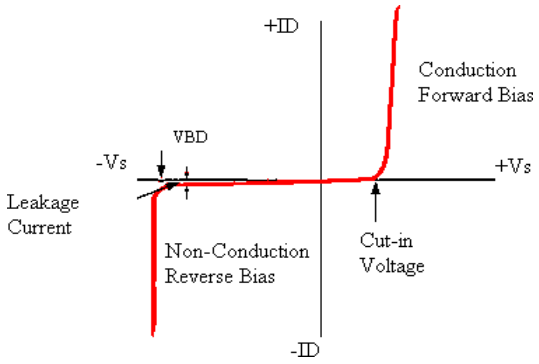


Figure (5): V-I Characteristics of P-N Junction Diode.

Figure (5) shows the V-I Characteristics of P-N Junction diode, V_S is the biasing voltage, I_D is the Diode Current and V_{BD} is the Break down voltage. The leakage current flows through the device under reverse biasing due to minority charge carriers. Under forward biasing and biasing voltage is greater than or equal to the threshold voltage, the device then acts as a conducting material.

Diode Characteristic Parameters:

1. Reverse Resistance (R_r):

The ratio of Reverse biasing voltage to the reverse current is called Reverse resistance of the PN Junction Diode.

i.e., $R_r = \frac{V_R}{I_o}$; where, V_R is the Biasing voltage under reverse biasing, called as reverse voltage and I_o is the reverse leakage current.

2. Forward Resistance (R_f):

The ratio of Forward biasing voltage to the Forward current is called Forward resistance of the PN Junction Diode.

i.e., $R_r = \frac{V_F}{I_F}$; where, V_F is the Biasing voltage under Forward biasing, called as Forward voltage and I_D is the Forward Current.

Diode Current Equation:

The diode current equation is given by,

$I_D = I_O(e^{\frac{V_F}{yV_T}} - 1)$

Where,

I_D is the diode current,

I_O is the reverse saturation or leakage current,

V_F is the applied forward voltage,

η is a constant 1 for Ge and 2 for Si and

V_T is the volt equivalent temperature (Thermal Voltage) is given by, $\boldsymbol{V_T = \frac{kT}{q}}$;

Where,

k is the boltzmann's constant,

T is the temperature in Kelvin and

q is the charge of an electron.

$$\boldsymbol{k = 1.38064852 \times 10^{-23}\, J/K}$$

$$\boldsymbol{q = 1.6x10^{-19} Coloumbs}$$

At room Temperature, i.e., at 300°K,

$$\boldsymbol{V_T = 25.85mV \approx 26mV}$$

$$V_T = \frac{\text{Or}}{\text{T}}{11600}$$

Equivalent Circuit of diode:

1. DC Equivalent Circuit.

The DC equivalent circuit of a diode under reverse biasing is an open circuit or Reverse Resistance R_r(typically in terms of MΩ) shown in figure (6a), and under forward biasing as shown in figure (6). Where R_f is the forward resistance of the diode, V_{ON} is the voltage drop across the diode under Conduction State (V_{ON}=0.7V for Silicon diodes and V_{ON}=0.3V for Germanium Diodes).

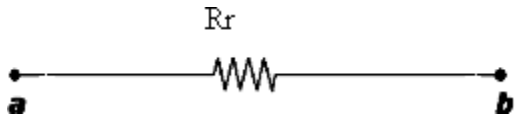


Figure (6a): Diode DC Equivalent Circuit under reverse biasing.

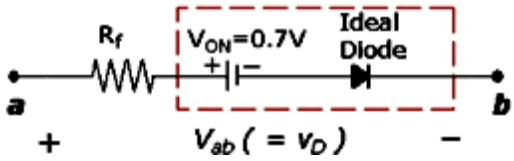


Figure (6b): Diode DC Equivalent Circuit under forward biasing.

2. AC Equivalent Circuit.

The AC equivalent circuit of a diode under reverse biasing and for forward biasing is the parallel connection of a Resistor and a Capacitor as shown in figure (7a) and figure (7b) respectively.

Under reverse biasing the depletion layer width increases and acts as a parallel plate capacitor with dielectric, hence the diode will be considered as a capacitor called Transition Capacitance/ Junction Capacitance/ Space charge Capacitance.

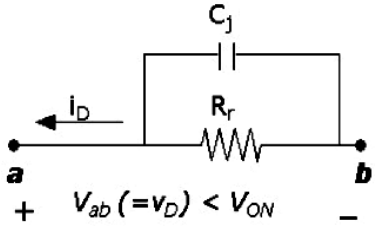


Figure (7a): AC Equivalent circuit under Reverse Biasing.

Under forward biasing the rate of change of charge carriers increases with respect to the applied forward voltage, hence the diode under forward biasing acts as a capacitor called diffusion Capacitance.

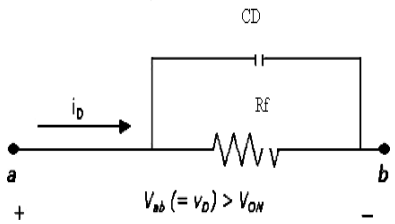


Figure (7b): AC equivalent Circuit under forward biasing.

Effect of Temperature on Diodes:

The number of charge carriers will vary depending on the temperature. i.e., if temperature increases the number of charge carriers also increases and due to this the conduction current (ID) also increases. The relation between current, voltage and temperature is as follows.

- The reverse saturation current doubles for every 10oC rise in Temperature.

$$\text{i.e., } I_O' = I_O \, x \, 2^{\left(\frac{t_2 - t_1}{10}\right)} \; ;$$

where,

I_O' is the reverse saturation current at temperature t_2 and
I_O is the reverse saturation current at temperature t_1.

- The forward voltage drop across the diode reduces 2.56mV for every 1°C rise in temperature.

$$\text{i.e., } V_F' = V_F - 2.56m(t_2 - t_1).$$

Where,

V_F' is the voltage drop across the diode at t2 and
V_F is the voltage drop across the diode at t1

Rectifiers:

Rectifiers are the electronics circuits that convert AC quantity into to DC quantity. This can be achieved by using unidirectional conduction devices like diode.

Depending on the conduction angle the rectifier circuits are classified into two types, they are,

1. Half wave Rectifier and
2. Full wave Rectifier.

The Full wave Rectifiers are further classified (based on number of diodes using) into two types, they are,

a. Center Tap Transformer (Two Diodes) full wave rectifier and
b. Bridge Type (Four Diodes) full wave rectifier.

1. Half wave Rectifier:

The half rectifier is an electronic circuit, which converts AC quantity into pulsating DC, by using a single diode with conduction angle only 180° that is only half cycle.

Circuit Diagram:

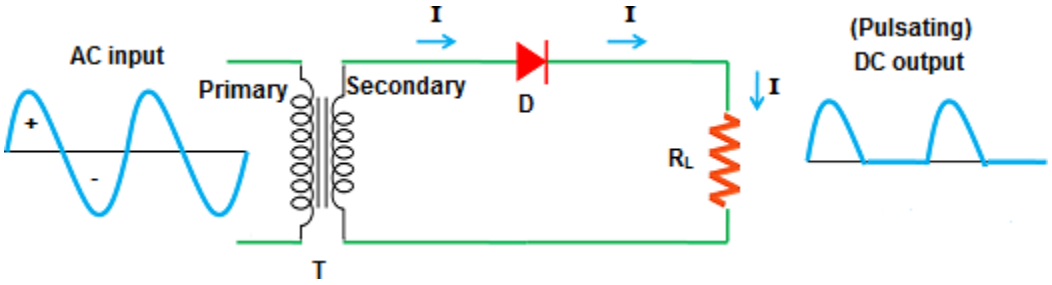


Figure (8): Half wave Rectifier circuit.

Figure (8) shows the circuit diagram of a half wave rectifier, where D is a diode (Assume Diode is ideal), R_L is the load resistor, input is an AC signal and output is the Pulsating DC Signal.

Explanation:

During every Positive half cycle diode D conducts and acts as a short circuit, hence the current flows through the Load resistor and is proportional to the input voltage according to Ohm's law, therefore the voltage across R_L is same as input signal.

i.e., $\boldsymbol{V_o = V_i}$

During every negative half cycle diode D does not conducts and acts as an open circuit and no current flows through the load element, hence the voltage across R_L is zero.

i.e., $\boldsymbol{V_o = 0}$

Waveforms:

Figure (9) shows the waveforms of an half wave rectifier circuit, and it can be observed that the output is only half cycle for every complete cycle input and also pulsating DC (Ripples/ some AC Components also present), i.e., not a pure DC.

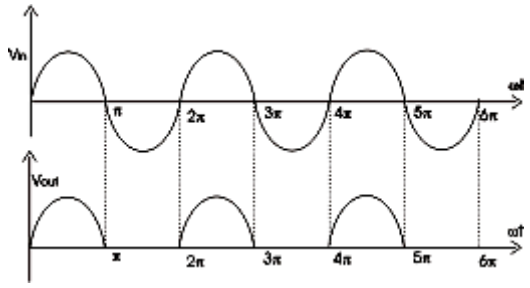


Figure (9): Input and Output Waveforms of a Half wave Rectifier circuit.

Mathematical expressions:

The output of half wave rectifier circuit is irregular in nature and hence, need to analyze the circuit for average DC and AC voltage or current along with the efficiency and ripple factor.

Transformer voltage and current is given by,

$\boldsymbol{v(t) = v_m sin mt}$.

$$\boldsymbol{i(t) = i_m sin mt}$$

Therefore

1. Average DC Voltage.

$$\boldsymbol{V_{dc} = \frac{1}{T}\int_0^T v(t)\,dmt}.$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_m sin mt\; dmt}.$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{\pi} v_m sin mt\; dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} v_m sin mt\; dmt}.$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{\pi} v_m sin mt\; dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} 0\; dmt}.$$

$$\boldsymbol{V_{dc} = \frac{v_m}{2\pi}[-cos mt]_0^{\pi}}$$

$$\boldsymbol{V_{dc} = \frac{v_m}{2\pi} x2}$$

$$\boldsymbol{V_{dc} = \frac{v_m}{\pi}}$$

2. Average DC Current.

$$I_{dc} = \frac{1}{T}\int_0^T I(t)dmt.$$

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_m sin mt\ dmt.$$

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i_m sin mt\ dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} i_m sin mt\ dmt\ .$$

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i_m sin mt\ dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} 0\ dmt\ .$$

$$I_{dc} = \frac{i_m}{2\pi}[-cos mt]_0^{\pi}$$

$$I_{dc} = \frac{i_m}{2\pi}x2$$

$$I_{dc} = \frac{i_m}{\pi}$$

Or

$$I_{dc} = \frac{V_{dc}}{R_L}$$

3. Root Mean Square value of the output voltage.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dmt}.$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (v_m sin mt)^2\ dmt}.$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} v^2{}_m sin^2\ mt\ dmt}.$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} v^2_m(1 - cos\ 2mt)/2\ \ dmt}.$$

$$V_{rms} = \frac{v_m}{2}$$

4. Root mean square value of the output current.

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dmt}.$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i_m sin mt)^2\ dmt}.$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2_m\ sin^2\ mt\ dmt}.$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} i^2{}_m(1 - cos\,2mt)/2 \;\; dmt.}$$

$$I_{rms} = \frac{i_m}{2}$$

Or

$$I_{rms} = \frac{V_{rms}}{R_L}$$

5. Ripple factor.

Ripple factor is the ratio of rms value of the ac component to the dc value of the component.

$$ripple\,factor\,(\gamma) = \frac{Vr_{rms}}{V_{dc}}$$

$$\gamma = \frac{\sqrt{V^2_{rms} - V^2_{dc}}}{V_{dc}}$$

$$\gamma = \frac{\sqrt{(\frac{V_m}{2})^2 - (\frac{V_m}{\pi})^2}}{\frac{V_m}{\pi}}$$

$$\gamma = 1.2114.$$

6. Efficiency.

It is the ratio of dc output power present in the output to the ac power input.

$$\eta = \frac{P_{dc}}{P_{ac}} x100$$

$$\eta = \frac{\frac{V^2_{dc}}{R_L}}{\frac{V^2_{rms}}{R_L}} x100$$

$$\eta = 0.406x100$$

$\eta = 40.6\%$.

7. Peak Inverse Voltage.

The maximum voltage applied across the diode under reverse biasing, in other words maximum reverse voltage, which occurs at the peak of the input signal when the diode is reverse biased is called Peak Inverse Voltage or Peak Reverse Voltage.

The Maximum reverse voltage applied across the diode is V_m.

i.e., $PIV = V_m$

Note: The above expressions holds good only for the ideal diode (R_f=0 and V_{ON}=0) and ideal transformer (R_s=0).

Case (i): For a diode with R_f.

$$I_m = \frac{V_m}{R_f + R_L}$$

$$I_{DC} = \frac{I_m}{\pi}$$

$$V_{DC} = I_{DC} X\, R_L$$

$$I_{rms} = \frac{I_m}{2}$$

$$V_{rms} = I_{rms} X\, R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_L)} x100$$

Case (ii): For a diode with R_f and Transformer with Rs

$$I_m = \frac{V_m}{R_f + R_s + R_L}$$

$$I_{DC} = \frac{I_m}{\pi}$$

$$V_{DC} = I_{DC} X\, R_L$$

$$I_{rms} = \frac{I_m}{2}$$

$$V_{rms} = I_{rms} X\, R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_s + R_L)} x100$$

Rectifier with C Filter:

From the above discussion it was observed that the output of the rectifier is not a pure dc. i.e., some ac components (ripples) also present, to remove the ripples we need to connect a filter. Filter can be capacitor or inductor, in the following context the capacitor filter will be discussed.

Filter is an electronic circuit which converts pulsating dc into pure dc.

The property of the capacitor is that it allows the ac component (High frequency component and low resistance) and blocks the dc component (low frequency component and high resistance).

Figure (10), shows the circuit diagram of an half-wave rectifier with capacitor filter, i.e., a capacitor is connected across the load resistor R_L. When AC voltage is applied, during the positive half cycle, the diode D is forward biased and allows electric current through it and capacitor starts charging instantly to its maximum level. During negative half cycle diode does not conducts and no current flow through the capacitor and hence starts discharging slowly. The discharging time constant is given by,

$$\boldsymbol{T_d = CR_L}$$

Note: If C or R_L or both increases the discharging time also increases and we will get pure dc. For very high Td the capacitor never discharges and it acts as a voltage source of value is equal to load voltage.

As we already know that, the capacitor provides high resistive path to dc components (low-frequency signal) and low resistive path to ac components (high-frequency signal).

Electric current always prefers to flow through a low resistance path. So when the electric current reaches the filter, the dc components experience a high resistance from the capacitor and ac components experience a low resistance from the capacitor.

The dc component does not like to flow through the capacitor (high resistance path). So they find an alternative path (low resistance path) and flows to the load resistor (RL) through that path shown in figure (11).

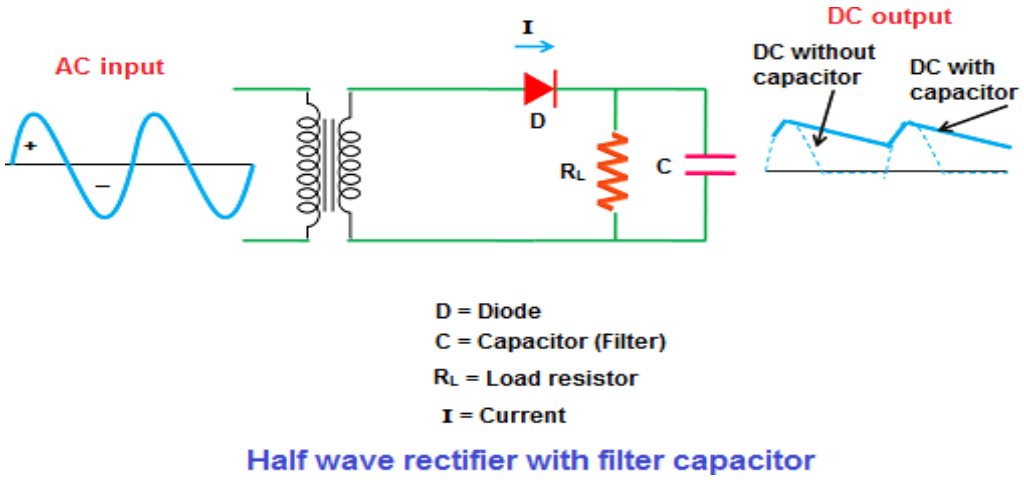


Figure (10): Half wave Rectifier circuit with Capacitor Filter.

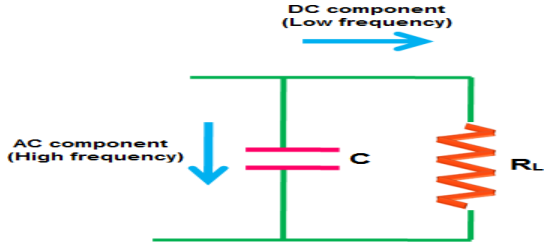


Figure (11): Working of Capacitor filter.

Electric current always prefers to flow through a low resistance path. So the AC components will flow through the capacitor whereas the DC components are blocked by the capacitor. Therefore, they find an alternate path and reach the output load resistor R_L. The flow of AC components through the capacitor is nothing but the charging of a capacitor.

Waveforms:

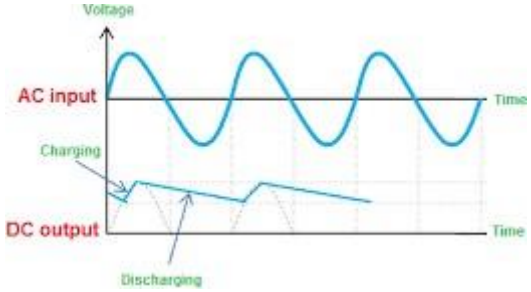


Figure (12): waveform of a Half wave Rectifier with C-filter.

Figure (12) shows the waveform of a half-wave rectifier filtered output. If discharging time increases then the output become pure dc.

The Ripple factor of a filtered output signal is given by

$$\gamma = \frac{1}{2\sqrt{3}fR_LC}$$

Advantage:

- Simple and easy to construct.
- PIV is only V_m.

Disadvantages:

- Conducts only half cycle, due to this more power will be wasted.
- More ripples occur in the output.

2. Full wave Rectifier using Center tap transformer:

A full wave rectifier is a type of rectifier which converts both half cycles of the AC signal into pulsating DC signal.

Circuit Diagram:

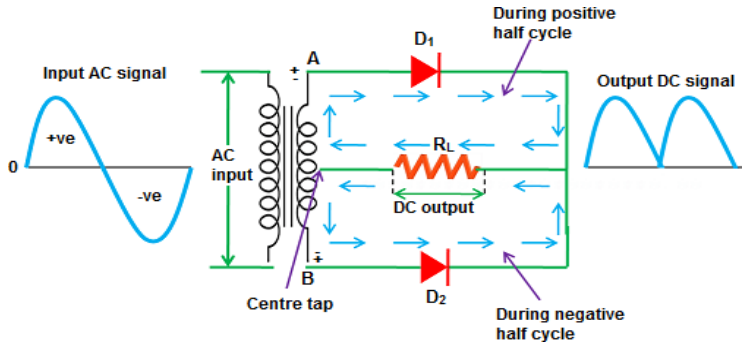


Figure (13): Full-wave Rectifier circuit.

As shown in the figure (13), the full wave rectifier converts both positive and negative half cycles of the input AC signal into output pulsating DC signal.

Note: The center tapped transformer shown in figure (14), works almost similar to a normal transformer. Like a normal transformer, the center tapped transformer also increases or reduces the AC voltage. However, a center tapped transformer has another important feature. That is the secondary winding of the center tapped transformer divides the input AC current or AC signal (V_P) into two parts.

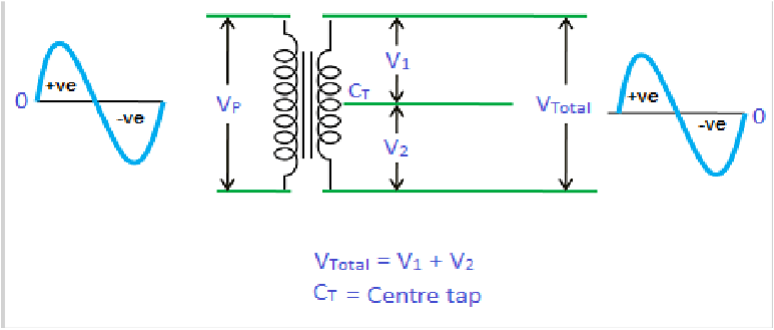


Figure (14): Working of Center Tapped Transformer.

The upper part of the secondary winding produces a positive voltage V_1 and the lower part of the secondary winding produces a negative voltage V_2. When we combine these two voltages at output load, we get a complete AC signal.

i.e. $\boldsymbol{V_{Total} = V_1 + V_2}$

The voltages V_1 and V_2 are equal in magnitude but opposite in direction. That is the voltages (V_1 and V_2) produced by the upper part and lower part of the secondary winding are 180 degrees out of phase with each other. However, by using a full wave rectifier with center tapped transformer, we can produce the voltages that are in phase with each other. In simple words, by using a full wave rectifier with center tapped transformer, we can produce a current that flows only in single direction.

The AC source is connected to the primary winding of the center tapped transformer. A center tap (additional wire) connected at the exact middle of the the secondary winding divides the input voltage into two parts.

The upper part of the secondary winding is connected to the diode D_1 and the lower part of the secondary winding is connected to the diode D_2. Both diode D_1 and diode D_2 are connected to a common load R_L with the help of a center tap transformer. The center tap is generally considered as the ground point or the zero voltage reference point.

Explanation:

The center tapped full wave rectifier uses a center tapped transformer and two diodes to convert the input AC voltage into output DC voltage.

When input AC voltage is applied, the secondary winding of the center tapped transformer divides this input AC voltage into two parts: positive and negative.

During every positive half cycle of the input AC signal, terminal A become positive, terminal B become negative and center tap is grounded (zero volts). The positive terminal A is connected to the p-side of the diode D_1 and the negative terminal B is connected to the n-side of the diode D_1. So the diode D_1 is forward biased during the positive half cycle and allows electric current through it.

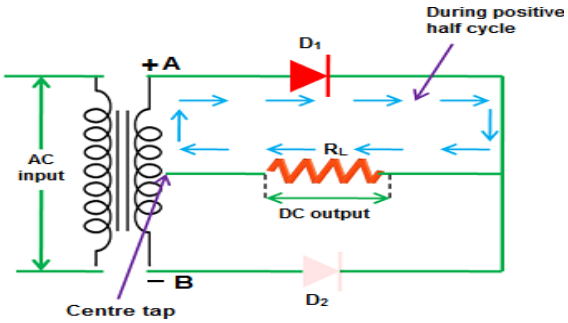


Figure (15): Full-wave rectifier circuit during every positive half cycle.

On the other hand, the negative terminal B is connected to the p-side of the diode D_2 and the positive terminal A is connected to the n-side of the diode D_2. So the diode D_2 is reverse biased during every positive half cycle and does not allow electric current through it.

The diode D_1 supplies DC current to the load R_L. The DC current produced at the load R_L will return to the secondary winding through a center tap.

i.e., $\boldsymbol{V_o = V_i}$

During the positive half cycle, current flows only in the upper part of the circuit while the lower part of the circuit carry no current to the load because the diode D_2 is reverse biased. Thus, during the positive half cycle of the input AC signal, only diode D_1 allows electric current while diode D_2 does not allow electric current as shown in figure (15).

During every negative half cycle of the input AC signal, terminal A become negative, terminal B become positive and center tap is grounded (zero volts). The negative terminal A is connected to the p-side of the diode D_1 and the positive terminal B is connected to the n-side of the diode D_1. So the diode D_1 is reverse biased during the negative half cycle and does not allow electric current through it.

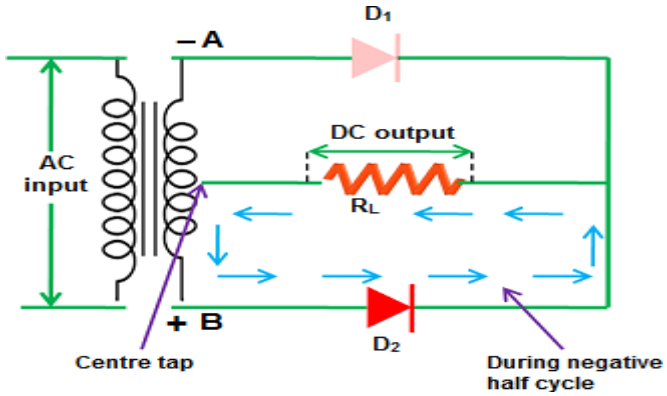


Figure (16): Full-Wave Rectifier during every negative half cycle.

On the other hand, the positive terminal B is connected to the p-side of the diode D_2 and the negative terminal A is connected to the n-side of the diode D_2. So the diode D_2 is forward biased during the negative half cycle and allows electric current through it.

The diode D_2 supplies DC current to the load R_L. The DC current produced at the load R_L will return to the secondary winding through a center tap as shown in figure (16).

During the negative half cycle, current flows only in the lower part of the circuit while the upper part of the circuit carry no current to the load because the diode D_1 is reverse biased. Thus, during the negative half cycle of the input AC signal, only diode D_2 allows electric current while diode D_1 does not allow electric current.

Thus, the diode D_1 allows electric current during the positive half cycle and diode D_2 allows electric current during the negative half cycle of the input AC signal. As a result, both half cycles (positive and negative) of the input AC signal are allowed. So the output DC voltage is almost equal to the input AC voltage as shown in figure (17).

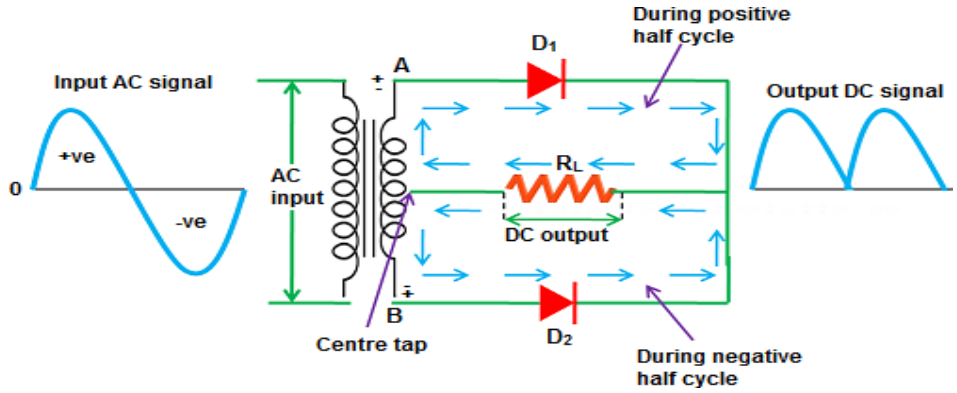


Figure (17): Full-wave rectifier with total output.

The diodes D_1 and D_2 are commonly connected to the load R_L. So the load current is the sum of individual diode currents.

We know that a diode allows electric current in only one direction. From the figure (17), we can see that both the diodes D_1 and D_2 are allowing current in the same direction.

We know that a current that flows in only single direction is called a direct current. So the resultant current at the output (load) is a direct current (DC). However, the direct current appeared at the output is not a pure direct current but a pulsating direct current.

The value of the pulsating direct current changes with respect to time. This is due to the ripples in the output signal. These ripples can be reduced by using filters such as capacitor and inductor.

The average output DC voltage across the load resistor is double that of the single half wave rectifier circuit.

Waveforms:

The output waveforms of the full wave rectifier is shown in figure (18).

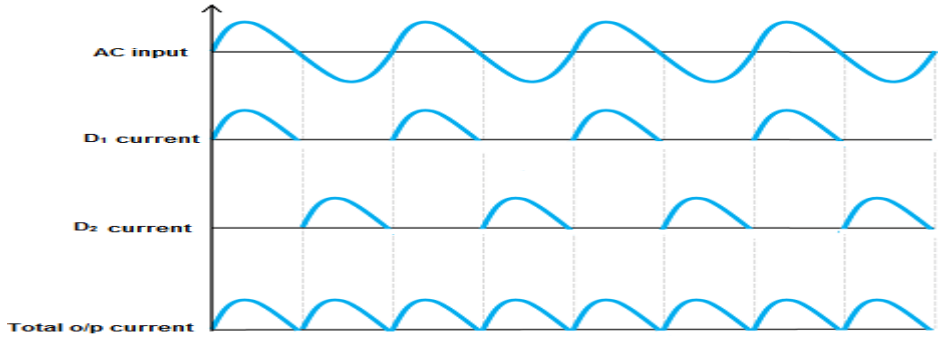


Figure (18): waveforms of full wave rectifier.

The first waveform represents an input AC signal. The second waveform and third waveform represents the DC signals or DC current produced by diode D_1 and diode D_2. The last waveform represents the total output DC current produced by diodes $D_1$and D_2. From the above waveforms, we can conclude that the output current produced at the load resistor is not a pure DC but a pulsating DC.

Mathematical Expressions:

The output of half wave rectifier circuit is irregular in nature and output would be equal to the average voltage or current.

Transformer voltage and current is given by,

$\boldsymbol{v(t) = v_m sin mt}$.

$$\boldsymbol{i(t) = i_m sin mt}$$

Therefore

1. Average or DC Voltage.

$$\boldsymbol{V_{dc} or\, V_{avg} = \frac{1}{T}\int_0^T v(t)\, dmt.}$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_m sin mt\; dmt.}$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{\pi} v_m sin mt\; dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} v_m sin mmt\; dt\,.}$$

$$\boldsymbol{V_{dc} = \frac{1}{2\pi}\int_0^{\pi} v_m sin mt\; dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} v_m sin mt\; dmt\,.}$$

Component Between π to $2\boldsymbol{\pi}$ is same as the 0 to π component.

Therefore,

$$\boldsymbol{V_{dc} = 2x\frac{1}{2\pi}\int_0^{\pi} v_m sin mt\; dmt.}$$

$$\boldsymbol{V_{dc} = 2x\frac{v_m}{2\pi}[-cos mt]_0^{\pi}}$$

$$\boldsymbol{V_{dc} = 2x\frac{v_m}{2\pi}x2}$$

$$\boldsymbol{V_{dc} = \frac{2v_m}{\pi}}$$

2. Average or DC Current.

$$I_{dc} or\ I_{avg} = \frac{1}{T}\int_0^T I(t)dmt.$$

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_m sinmt\ dmt.$$

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i_m sinmt\ dmt + \frac{1}{2\pi}\int_{\pi}^{2\pi} i_m sinmt\ dmt\ .$$

$$I_{dc} = 2x\frac{1}{2\pi}\int_0^{\pi} i_m sinmt\ dmt$$

$$I_{dc} = 2x\frac{i_m}{2\pi}[-cosmt]_0^{\pi}$$

$$I_{dc} = 2x\frac{i_m}{2\pi}x2$$

$$I_{dc} = \frac{2i_m}{\pi}$$

Or

$$I_{dc} = \frac{V_{dc}}{R_L}$$

3. Root Mean Square value of the output voltage.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dmt.}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (v_m sinmt)^2\ dmt.}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v_m^2 sin^2\ mt\ dmt.}$$

$$V_{rms} = \sqrt{2x\ \frac{1}{2\pi}\int_0^{\pi} v_m^2(1 - cos\ 2mt)/2\ \ dmt.}$$

$$V_{rms} = \frac{v_m}{\sqrt{2}}$$

4. Root mean square value of the output current.

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dmt.}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i_m sinmt)^2\ dmt.}$$

$$I_{rms} = \sqrt{2x\frac{1}{2\pi}\int_0^{\pi} i^2{}_m sin^2\ mt\ dmt.}$$

$$I_{rms} = \sqrt{2x\ \frac{1}{2\pi}\int_0^{2\pi} i_m^2\ (1 - cos\ 2mt)/2\ \ dmt.}$$

$$I_{rms} = \frac{i_m}{\sqrt{2}}$$

Or

$$I_{rms} = \frac{V_{rms}}{R_L}$$

5. Ripple factor.

Ripple factor is the ratio of rms value of the ac component to the dc value of the component.

$$\textbf{ripple factor (y)} = \frac{\mathbf{Vr_{rms}}}{\mathbf{V_{dc}}}$$

$$y = \frac{\sqrt{\mathbf{V^2_{rms}} - \mathbf{V^2_{dc}}}}{\mathbf{V_{dc}}}$$

$$y = \frac{\sqrt{\left(\frac{\mathbf{V_m}}{\sqrt{\mathbf{2}}}\right)^2 - \left(\frac{\mathbf{2V_m}}{\boldsymbol{\pi}}\right)^2}}{\frac{\mathbf{2V_m}}{\boldsymbol{\pi}}}$$

$y = \mathbf{0.48}$.

6. Efficiency.

It is the ratio of dc output power present in the output to the ac power input.

$$\eta = \frac{\mathbf{P_{dc}}}{\mathbf{P_{rms}}}\mathbf{x100}$$

$$\eta = \frac{\frac{\mathbf{V^2_{dc}}}{\mathbf{R_L}}}{\frac{\mathbf{V^2_{rms}}}{\mathbf{R_L}}}\mathbf{x100}$$

$$\eta = \mathbf{0.812x100}$$

$\eta = \mathbf{81.2\%}$.

7. Peak Inverse Voltage.

The maximum voltage applied across the diode under reverse biasing, in other words maximum reverse voltage, which occurs at the peak of the input signal when the diode is reverse biased is called Peak Inverse Voltage or Peak Reverse Voltage.

The Maximum reverse voltage applied across the diode is $2V_m$.

i.e., $\boldsymbol{PIV = 2V_m}$

Note: The above expressions holds good only for the ideal diode (R_f=0 and V_{ON}=0) and ideal transformer (R_s=0).

Case (i): For a diode with R_f.

$$I_m = \frac{V_m}{R_f + R_L}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} X\, R_L$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = I_{rms} X\, R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_L)} x100$$

Case (ii): For a diode with R_f and Transformer with Rs

$$I_m = \frac{V_m}{R_f + R_s + R_L}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} X R_L$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = I_{rms} X R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_s + R_L)} x100$$

Full-wave Rectifier with C Filter:

The filter is an electronic device that converts the pulsating Direct Current into pure Direct Current.

In the circuit diagram, the capacitor C is placed across the load resistor R_L.

Note: The working of the full-wave rectifier with filter is almost similar to that of the half wave rectifier with filter. The only difference is that in the half wave rectifier only one half cycles (either positive or negative) of the input AC current will charge the capacitor but the remaining half cycle will not charge the capacitor. But in full wave rectifier, both positive and negative half cycles of the input AC current will charge the capacitor.

The main duty of the capacitor filter is to short the ripples to the ground and blocks the pure DC (DC components), so that it flows through the alternate path and reaches output load resistor R_L.

Figure (19) shows the circuit diagram of a full-wave rectifier with Capacitor filter, when input AC voltage is applied, during the positive half cycle, the diode D_1 is forward biased and allows electric current whereas the diode D_2 is reverse biased and blocks electric current. On the other hand, during the negative half cycle the diode D_2 is forward biased (allows electric current) and the diode D_1 is reverse biased (blocks electric current).

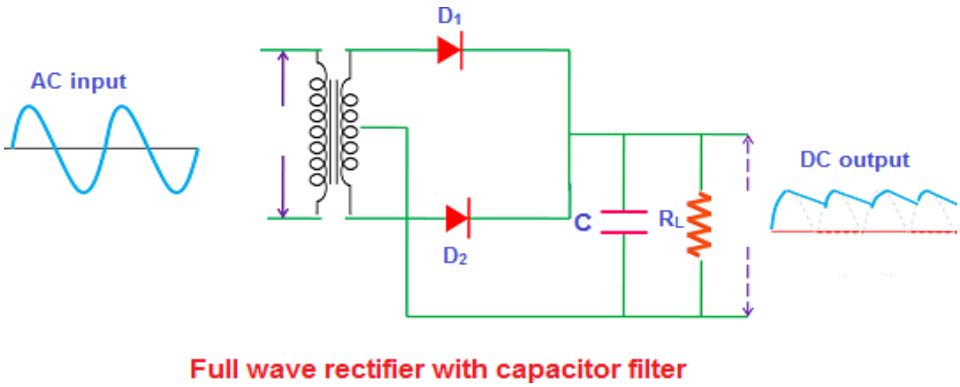


Figure (19): Full-wave Rectifier circuit with Capacitor filter.

During the positive half cycle, the diode (D_1) current reaches the filter and charges the capacitor. However, the charging of the capacitor happens only when the applied AC voltage is greater than the capacitor voltage.

Initially, the capacitor is uncharged. That means no voltage exists between the plates of the capacitor. So when the voltage is turned on, the charging of the capacitor happens immediately.

During this conduction period, the capacitor charges to the maximum value of the input supply voltage. The capacitor stores a maximum charge exactly at the quarter positive half cycle in the waveform. At this point, the supply voltage is equal to the capacitor voltage.

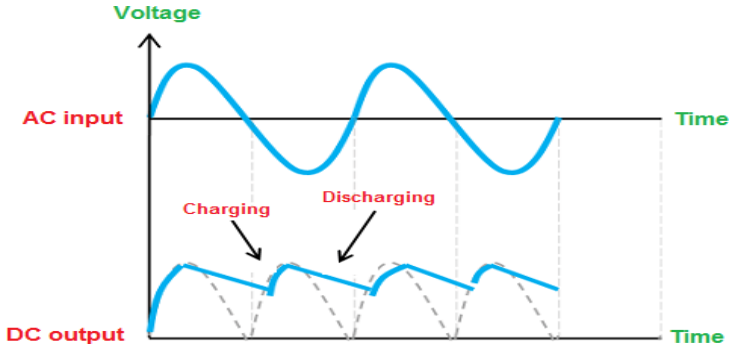


Figure (20): Full-wave Rectifier filtered output.

When the AC voltage starts decreasing and becomes less than the capacitor voltage, then the capacitor starts slowly discharging as shown in figure (20).

The discharging of the capacitor is very slow as compared to the charging of the capacitor. So the capacitor does not get enough time to completely discharge. Before the complete discharge of the capacitor happens, the charging again takes place. So only half or more than half of the capacitor charge get discharged.

When the input AC supply voltage reaches the negative half cycle, the diode D_1 is reverse biased (blocks electric current) whereas the diode D_2 is forward biased (allows electric current). During the negative half cycle, the diode (D_2) current reaches the filter and charges the capacitor. However, the charging of the capacitor happens only when the applied AC voltage is greater than the capacitor voltage.

The capacitor is not completely uncharged, so the charging of the capacitor does not happen immediately. When the supply voltage becomes greater than the capacitor voltage, the capacitor again starts charging.

In both positive and negative half cycles, the current flows in the same direction across the load resistor R_L. So we get either complete positive half cycles or negative half cycles. In our case, they are complete positive half cycles.

The Ripple factor of a filtered output signal is given by

$$\gamma = \frac{1}{4\sqrt{3} f R_L C}$$

Advantages:

- Conducts both the half cycles.
- Efficiency is improved
- Ripples factor is reduced.

Disadvantages:

- Center tapped transformer more expensive and bulky.
- PIV is 2Vm.

3. Bridge type Full wave Rectifies:

The Bridge Type Full-wave rectifier is an electronic circuit, which converts AC quantity into pulsating DC, by using the four diodes with conduction angle only 360^o that is complete cycle.

Circuit Diagram:

The Circuit diagram of a bridge rectifier is shown in figure (21). The bridge rectifier is made up of four diodes namely D_1, D_2, D_3, D_4 and load resistor R_L. The four diodes are connected in a closed loop (Bridge) configuration to efficiently convert the Alternating Current (AC) into Direct Current (DC).

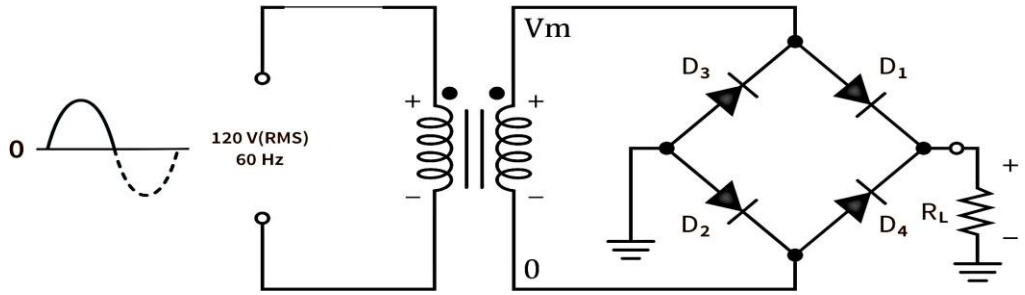


Figure (21): Full-wave Bridge Rectifier Circuit diagram.

Explanation:

The input AC signal is applied across two terminals A and B and the output DC signal is obtained across the load resistor R_L which is connected between the terminals C and D.

The four diodes D_1, D_2, D_3, D_4 are arranged in series with only two diodes allowing electric current during each half cycle. For example, diodes D_1 and D_2 are considered as one pair which allows electric current during the positive half cycle whereas diodes D_3 and D_4 are considered as another pair which allows electric current during the negative half cycle of the input AC signal.

When input AC signal is applied across the bridge rectifier, during the positive half cycle diodes D_1 and D_2 are forward biased and allows electric current while the diodes D_3 and D_4 are reverse biased and blocks electric current. On the other hand, during the negative half cycle diodes D_3 and D_4 are forward biased and allow electric current while diodes D_1 and D_2 are reverse biased and blocks electric current.

During the positive half cycle, the terminal A becomes positive while the terminal B becomes negative. This causes the diodes D_1 and D_2 forward biased and at the same time, it causes the diodes D_3 and D_4 reverse biased.

The current flow direction during the positive half cycle is shown in the figure (22) (i.e. A to D to C to B).

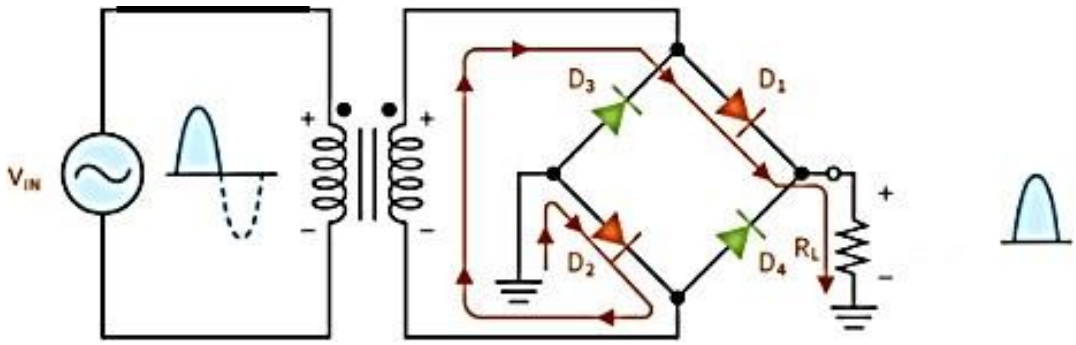


Figure (22): Bridge Rectifier during every positive half cycle.

During the negative half cycle, the terminal B becomes positive while the terminal A becomes negative. This causes the diodes D_3 and D_4 forward biased and at the same time, it causes the diodes D_1 and D_2reverse biased.
The current flow direction during negative half cycle is shown in figure (23) (I.e. B to D to C to A).

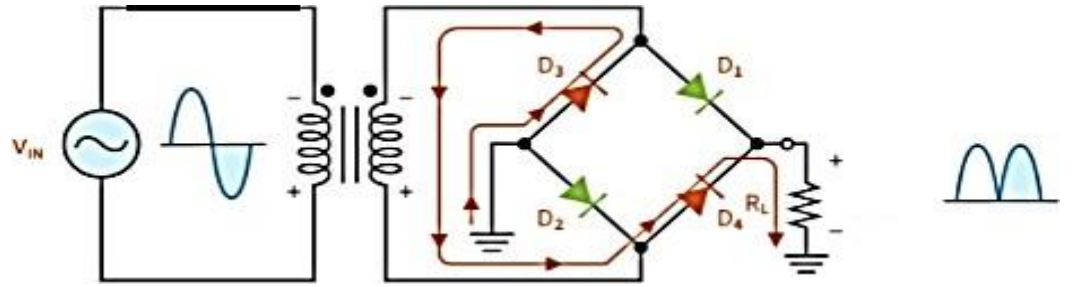


Figure (23): Bridge Rectifier during every negative half cycle.

From the two figures (22 and 23), we can observe that the direction of current flow across load resistor R_L is same during the positive half cycle and negative half cycle. Therefore, the polarity of the output DC signal is same for both positive and negative half cycles. The output DC signal polarity may be either completely positive or negative. In our case, it is completely positive. If the direction of diodes is reversed then we get a complete negative DC voltage.
Thus, a bridge rectifier allows electric current during both positive and negative half cycles of the input AC signal.
The output waveforms of the bridge rectifier is shown in figure (24).

Waveforms:

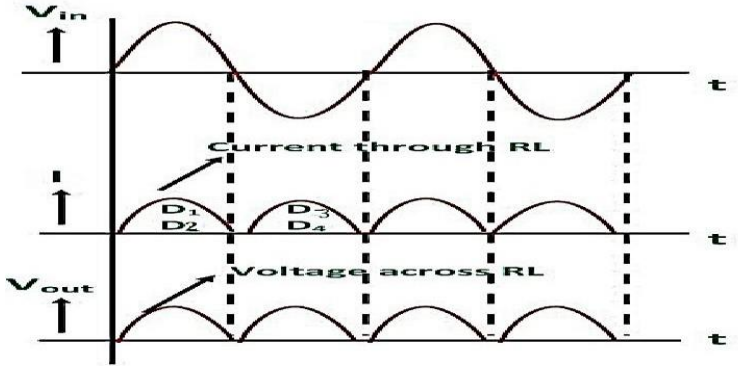


Figure (24): Bridge Rectifier waveforms.

Mathematical Expressions:
Same as Full wave Rectifier except PIV.
PIV of Bridge type full wave rectifier is only Vm.

$$\text{i.e., } \boldsymbol{PIV = V_m}$$

Note: The above expressions holds good only for the ideal diode (R_f=0 and V_{ON}=0) and ideal transformer (R_s=0).
Case (i): For a diode with R_f.

$$I_m = \frac{V_m}{2R_f + R_L}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} X\, R_L$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = I_{rms} X\, R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (2R_f + R_L)} x100$$

Case (ii): For a diode with R_f and Transformer with Rs

$$I_m = \frac{V_m}{2R_f + R_s + R_L}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} X\, R_L$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = I_{rms} X\, R_L$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

$$\%\eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (2R_f + R_s + R_L)} x100$$

Bridge Rectifier with C Filter:
Same as Full wave Rectifier with C Filter.

Advantages:
- Center tapped Transformer is not necessary hence circuit becomes simple and cheap.
- PIV is only Vm.

Disadvantages:
- Requires four diodes.

Choke Filter:

Choke filter is a circuit consists of an inductor connected in series with load and capacitor connected across the load. The choke filter is also called L-section filter as shown in figure (25).

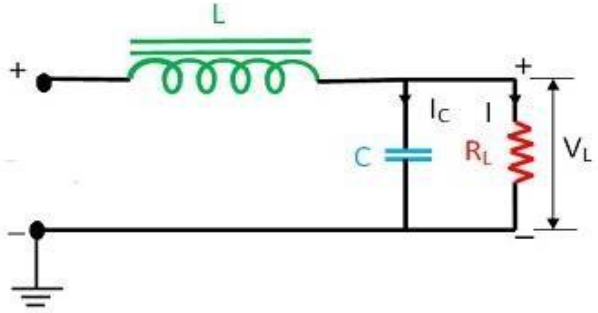


Figure (25): Choke Filter.

The choke filter is used to remove the ripples present in the rectified output. The Pulsating DC signal pass through the inductor or choke will blocks ac and allows dc and further the ripples i.e., some of the residual ripples will get bypassed through the capacitor (capacitor blocks dc and allows ac). Hence from the choke filtered output is pure dc.

The Ripple factor of a filtered output signal is given by

$$\gamma = \frac{1.19}{LC}$$

Significance of Choke filters:

The series inductor filter decreases the current, and shunt capacitor filter increases the current.

Zener Diode:

The reverse current through the normal diode is in terms of microamperes and it is almost constant until the reverse voltage is less than break down voltage, if the reverse voltage is greater than or equal to the break down voltage the junction breaks and high current will flow through the device and more power will be dissipated then the device may be destroyed or damaged.

If we limit the current through the device by means of connecting a resistor in series with the device, the power dissipation reduces and the device may not be destroyed even under breakdown region. By using this principle the special type of diode is designed by Clearance Zener called as Zener diode.

There are two types of breakdown occurs in Zener diode depending on the break down voltage levels.

i) Zener Break down:

This type of breakdown occurs in the device if the breakdown voltage is less than or equal to 6V(typically), this strong electric field at the junction becomes very large and breaks the covalent bonds to release free electrons, due to this very high current will flow through the device. This mechanism or process is called ionization by Electric field.

ii) Avalanche Breakdown:

This type of breakdown occurs in the device if the breakdown voltage is greater than 6V (Typically), this high potential forces minority charge carriers to move quickly means kinetic energy increases, due to this the minority charge carriers collide with atoms to break covalent bonds which increase the free electrons and hence the current increases sharply. This process or mechanism is called, Impact Ionization or Ionization by collision. In this mechanism, the free electrons increase in multiples and hence called avalanche breakdown.

VI Characteristics of Zener Diode:

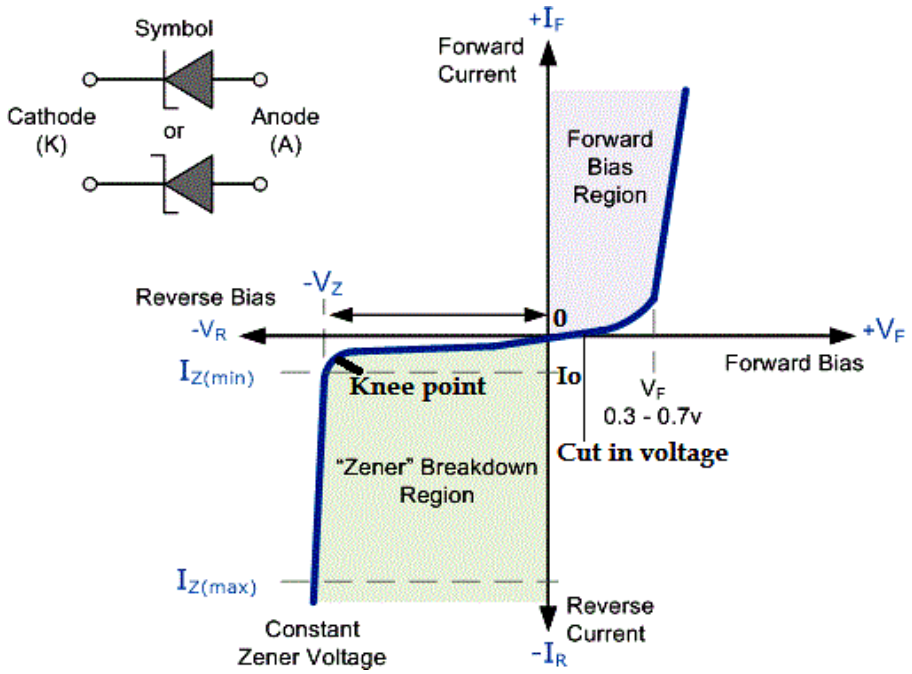


Figure (26): VI Characteristics of Zener Diode.

Zener Diode Voltage Regulator:

Zener diode provides constant voltage if the Zener Current is between I_{Zmin} to I_{Zmax} under reverse biasing, this feature of Zener diode will be utilized to design a voltage regulator.

Voltage regulator is a system which produces the constant voltage irrespective of variations in line (Input) and load.

Figure (27) shows the circuit diagram of a Zener Diode Voltage Regulator. Where, R is the Series Resistor used to limit or control the sharp current flowing through the Zener diode under breakdown condition, R_L is the Load resistance, V_i is the unregulated power supply, I_Z is the current through the Zener diode, I_L is the load current, V_R is the voltage drop across series resistor. V_Z is the Zener Voltage, V_o is the voltage across the load resistor called output voltage and I is the input current.

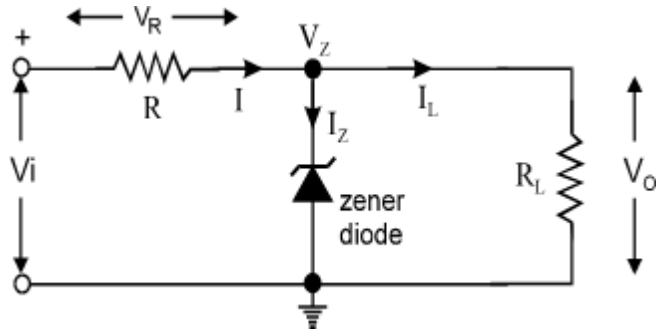


Figure (27): Zener Diode Voltage Regulator Circuit.

From the above figure, the input unregulated power supply V_i, Positive terminal is connected to the cathode terminal and negative terminal is connected to the anode terminal, hence the Zener diode is operating in the reverse biasing mode.

And the above circuit provides a constant voltage even by varying the input voltage and varying load, i.e., provides regulation for both line and load.

Case(i): Line Regulation; Variable input and constant load:

If the input voltage V_i is less than the Zener Voltage V_Z (Zener Break Down Voltage), the output voltage is same as the input voltage Vi, because the Zener diode is in off state, if the input voltage is greater than the Zener voltage V_Z, the diode in ON state and hence it acts as a voltage source of V_Z Volts.

If V_i increases, the input current I also increases, and I_Z increases to maintain I_L constant, but I_Z should be between I_{Zmin} to I_{Zmax}.

If V_i decreases, the input current I also decreases, and I_Z decreases to maintain I_L constant, but I_Z should be between I_{Zmin} to I_{Zmax}.

Therefore the voltage across the load resistor constant and is given by

$$V_o=V_Z$$

Case(ii): Load Regulation; Fixed input and variable load:

If R_L increases, I_L decreases and to keep input current I constant I_Z increases, but I_Z should be between I_{Zmin} to I_{Zmax}.

If R_L decreases, I_L increases and to keep input current I constant I_Z decreases, but I_Z should be between I_{Zmin} to I_{Zmax}.

Therefore the voltage across the load resistor constant and is given by

$$V_o=V_Z$$

Bipolar Junction Transistor.

Introduction:

Electronic systems are interconnection or combination of electronic devices and electrical elements. Electrical elements in the electronic systems are used to bias the electronic devices. Semiconductor devices such as diodes and transistors are called electronic devices. Electronic devices are used for switching and amplification purpose. Diodes are used for switching applications and they are not having the capability of amplifying the signals. Therefore diodes are limited to switching applications.

The transistor is a three-terminal device that can amplify the signals as well as performing switching action.

The term transistor is derived from the statement transfer of resistor that is a transistor will transfers the resistance from one junction to another junction through proper biasing. Hence, transistors perform amplification by changing their resistance.

Transistor
Transfer of Resistor

The first transistor was demonstrated on 23rd Dec 1947, by Dr. Willian Shockley and his team at the Bell Telephone Laboratories, USA

The important features of transistors compared to vacuum tubes are listed as follows.

1. Three terminal solid-state device
2. Smaller and lightweight
3. Rugged construction
4. No heater requirement
5. Requires less power
6. Lower operating voltage and
7. More efficient.

With these advantages, transistors are developed and used in all electronic systems as a switch and/or amplifier.

Classification:

Figure (1) shows the classification of transistors.

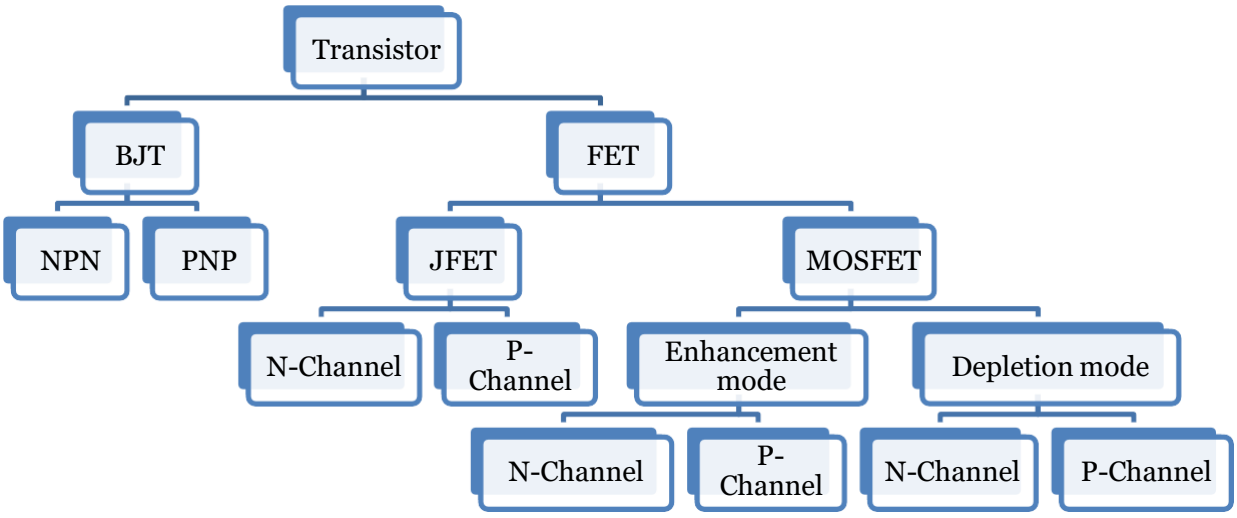


Figure 1: Classification of transistors.

In the following section, BJTs construction, working principle, characteristics and applications are discussed.

BJT, stands for bipolar junction transistor, figure (2) shows the structure of BJT and terminologies.

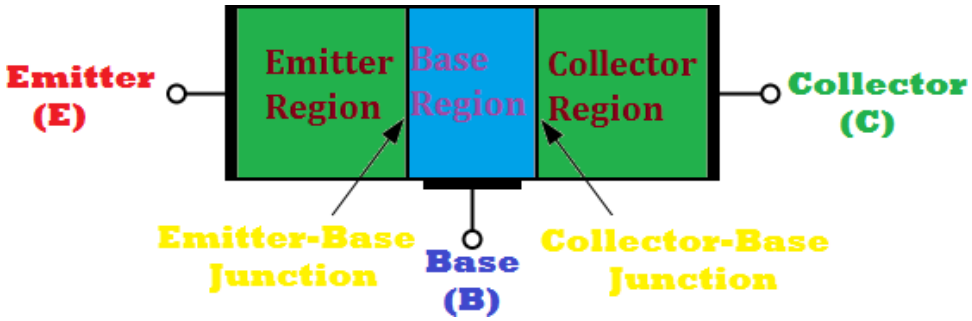


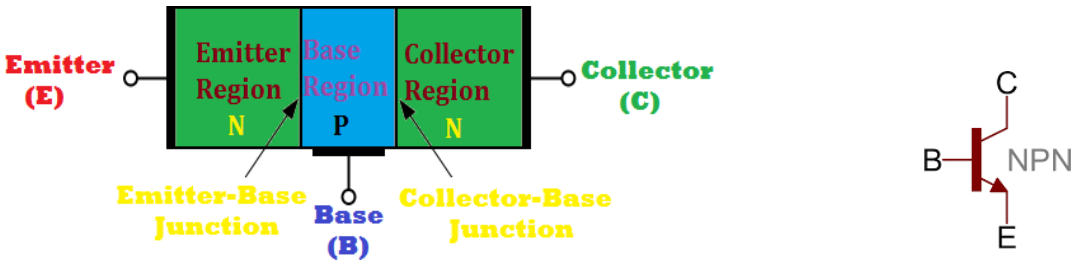
Figure 2: Structure of transistor.

- **Bipolar:** Both electrons and holes are involved in current flow.
- **Junction:** has two p-n junctions.
- **Transistor:** Transfer + Resistor.
  - BJTs are current-controlled devices
  - Have three regions with three terminals labeled as

i. Emitter (**E**)
ii. Base (**B**) and
iii. Collector (**C**)

Figure (3) shows the structure and circuit symbol of NPN and PNP transistors.

- **NPN- Bipolar Junction Transistor**



- **PNP- Bipolar Junction Transistor**
-

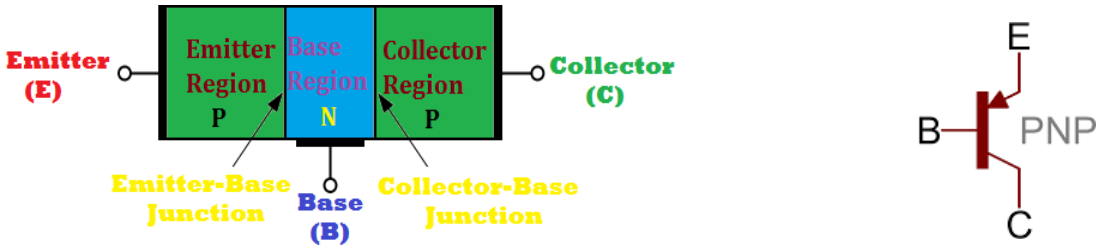


Figure 3: Structure and circuit symbols of NPN and PNP transistor.

The arrow in the circuit symbols indicates the direction of the current flow. In the NPN transistor, current will flow from collector to emitter terminal and in the PNP transistor current will flow from emitter to collector.

Construction:

In the following section, the step-by-step process of constructing NPN – BJT is explained, the following specifications are to be considered for constructing BJTs.

	Emitter	**Base**	**Collector**
Width	Medium	Thin	High
Doping Concentration	High	Low	Moderate

Step1: start with a piece of intrinsic semiconductor and divided it into three regions

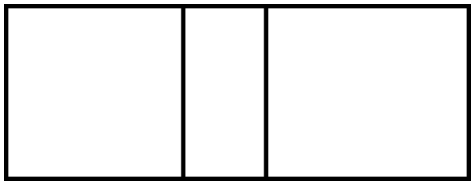


Figure 4: Piece of intrinsic semiconductor

Step2: Three regions are doped to form NPN regions

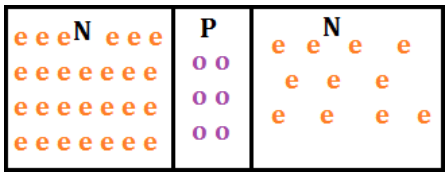


Figure 5: Doped intrinsic semiconductor

Doping with pentavalent element gives N-type material and doping with trivalent element gives P-type semiconductor material.

Step3: Metallic contacts are deposited at each layer to connect the electrodes to form terminals

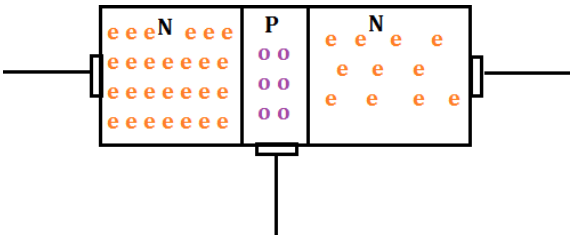


Figure 6: Electrodes connected to each layer

Step4: Terminals are named as Emitter, Base, and Collector

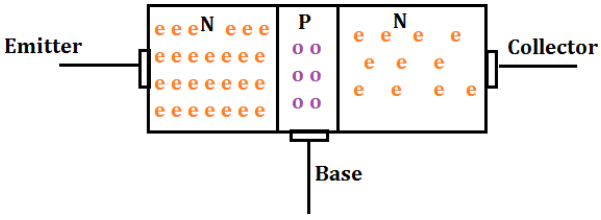


Figure 7: Terminals are named as emitter, base, and collector

The emitter terminal emits more electrons and hence, the emitter region is doped heavily, Collector terminal collects the emitted electrons, hence the width of the collector region is high.

The base terminal is a lightly doped and thin region, which controls the electrons flow from emitter to collector.

Working Principle:

The BJTs are working under three different modes, such as cut-off, saturation and active modes and the working principle of NPN-BJT is explained with these three modes.

Case (i): Cut-off mode

- Both Emitter-Base and Collector-Base junctions are reverse biased
- The depletion region widens at both the junctions and no current will flow through the device.
- Acts as an OFF switch

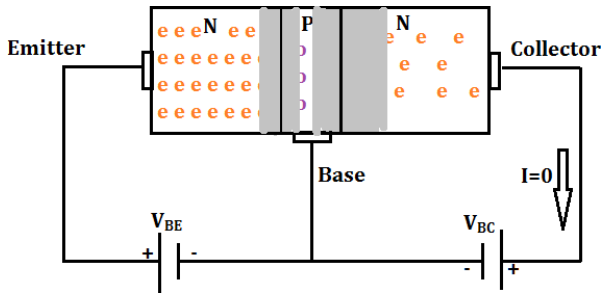


Figure 8: Cut-off mode operation of BJT

Case (ii): Saturation Mode

- Both Emitter-Base and Collector-Base junctions are forward biased
- The depletion region reduces at both the junctions and maximum current will flow through the device.
- Acts as an ON switch.

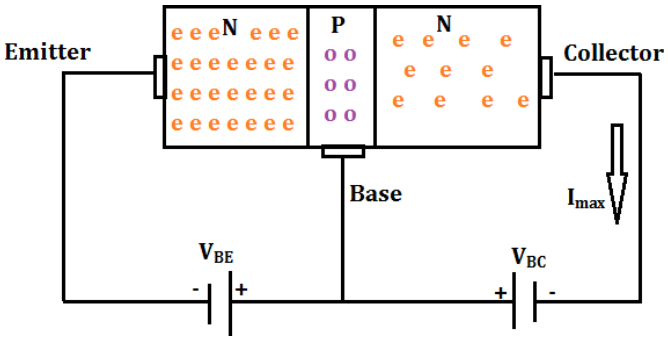


Figure 8: Saturation mode operation of BJT

Case (iii): Active Mode

- Emitter-Base Junction is forward biased and Collector-Base junction is reverse biased
- The width of the depletion region decreases at EB Junction.
- Width of the depletion region Increases at CB Junction.
- Electrons move through the base region, but the base region is lightly doped and only a few electrons recombine with the holes present in the base region, remaining electrons are drifted towards the collector region and constitute a collector current.
- Only 2-5% of electrons recombine at the base region, remaining 95 to 98% electrons move to the collector region
- Transfer of resistance takes place, hence it is called the transistor.
- Acts as an amplifier

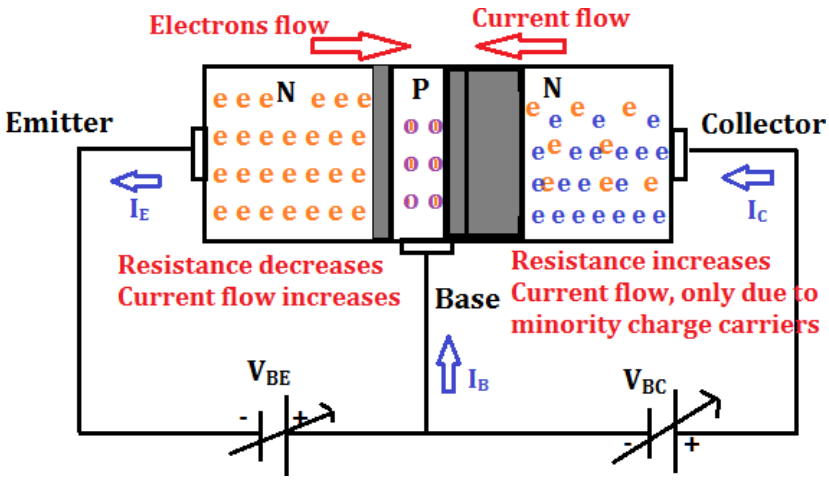


Figure 8: Active mode operation of BJT

Characteristics of BJT:

Bipolar junction transistor is a three-terminal device and BJTs are need to be modeled as a two-port network. A pair of terminals is called a port, the two-port network means, the network has two pairs of terminals. One pair of terminals used to apply the input and another pair of terminals is used to take the corresponding output. Figure (9) shows the block diagram of two-port model.

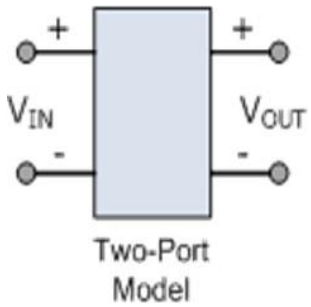


Figure 9: Two-port model

One terminal of BJT can be connected to the ground or made common to both input and output to form a two-port model, which leads to three different configurations they are.

1. Common Base (CB) Configuration
2. Common Emitter (CE) Configuration and
3. Common Collector (CC) Configuration.

Each of these configurations is having its advantages and disadvantages. To study the behavior of these configurations, VI characteristics need to be obtained, VI Characteristics of BJTs are divided into two types they are.

1. Input characteristics and
2. Output characteristics

1. Common Base (CB) Configuration:

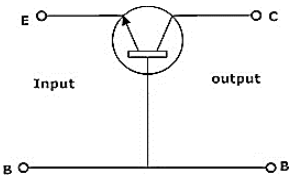


Figure 10: CB Configuration of NPN-BJT

- The base terminal(grounded) is common for both input and output
- Input is applied between E and B
- Output is taken across C and B
- I_E is the input current and I_C is the output current
- V_{EB} is the input voltage and V_{CB} is the output voltage

Where,

- I_E - Emitter current
- I_C - Collector current
- V_{EB} - Emitter to base voltage
- V_{CB} - collector to base voltage.

Figure (11) shows the circuit arrangement to obtain the VI characteristics

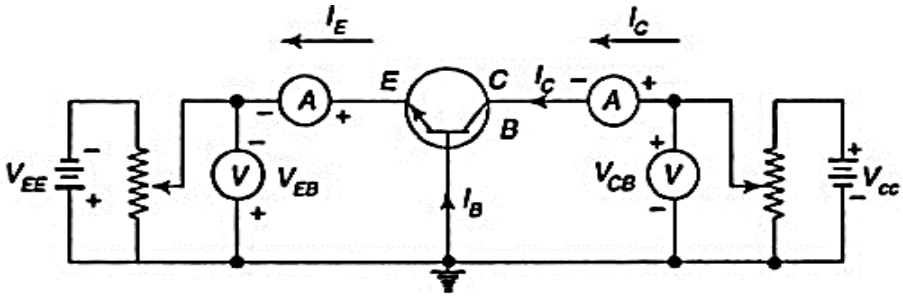


Figure 11: Circuit arrangement to obtain the VI Characteristics

Input Characteristics:

- V_{EB} vs I_E with zero or constant V_{CB}
- Initially, the collector-base voltage V_{CB} is kept at zero, and emitter current I_E is increased from zero by increasing V_{EB}.
- The EB junction depletion region reduces by increasing V_{EB} and if V_{EB} is greater than or equal to cut-in voltage, current starts increasing.
- This characteristic is similar to the forward bias characteristics of the diode.
- **Effect of V_{CB}:** If V_{CB} is increased, the depletion region of the CB junction increases and the depletion region penetrates deeper into the base region, which leads to a decrease in the width of the based region, so emitter current increases. **This effect is called early effect or based width modulation.**

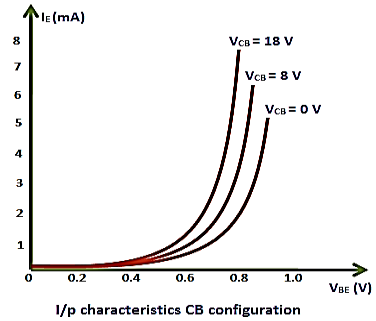


Figure 12: Input characteristics of CB configuration

Output Characteristics:

- V_{CB} vs I_C with zero or constant I_E
- If I_E is zero, and CB junction reverse-biased, a small current will flow through the device. This current is called reverse leakage current, denoted as I_{CBO}.
- If I_E increases by increasing V_{EB}, the emitter terminal injects more electrons and less recombination takes place at the base region due to early effect, and hence collector current increases proportionally to emitter current.
- i.e., $I_C = \alpha I_E + ICBO$; I_{CBO} is the leakage current and small
- $I_C = \alpha I_E$; α is the current amplification factor of CB configuration typically 0.95 to 0.98
- $I_C \approx I_E$; Collector current is approximately equal to emitter current.

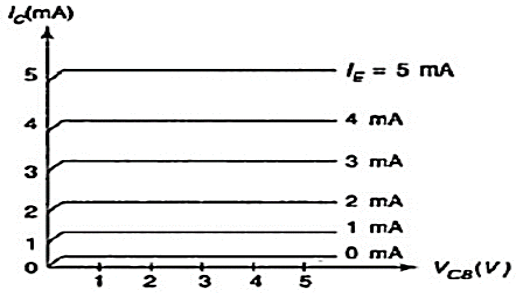


Figure 13 Output characteristics of CB configuration

Mathematical Expressions:

$$I_E = I_C + I_B - - - (1)$$
$$I_C = \alpha I_E + I_{CBO} - - - (2)$$
$$\alpha I_E \gg I_{CBO}$$
$$I_C = \alpha I_E$$

Where,

$$\alpha = \frac{\boldsymbol{I_C}}{\boldsymbol{I_E}}$$

$current\ amlification\ factor\ of\ CB\ configuration$

Typically

$\alpha = 0.95\ to\ 0.98$;

$$\boldsymbol{I_C \approx I_E}$$

2. Common Emitter (CE) Configuration

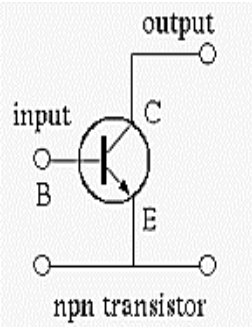


Figure 14: CE configuration

- Emitter terminal is common (grounded) for both input and output
- Input is applied between B and E
- Output is taken across C and E
- I_B is the input current and I_C is the output current
- V_{BE} is the input voltage and V_{CE} is the output voltage

Where,

- I_B – Base current

- I_C - Collector current
- V_{BE} – Base to Emitter voltage
- V_{CE} - collector to Emitter voltage

Figure (15) shows the circuit arrangement for obtaining the VI Characteristics

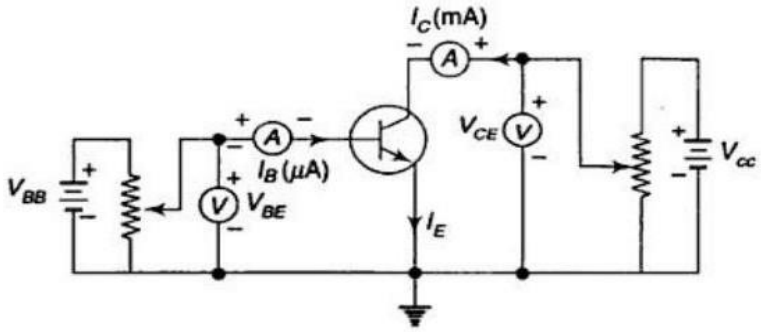


Figure 15: Circuit arrangement to obtain the characteristics.

Input characteristics

- V_{BE} vs I_B with zero or constant V_{CE}
- Initially, the collector-emitter voltage V_{CE} is kept at zero, and emitter current I_B is increased from zero by increasing V_{BE}.
- The EB junction depletion region reduces by increasing V_{BE} and if V_{BE} is greater than or equal to cut-in voltage, current starts increasing.
- This characteristic is similar to the forward bias characteristics of the diode.
- **Effect of V_{CE}:** If V_{CE} is increased, the depletion region of the CB junction increases and the depletion region penetrates deeper into the base region, which leads to a decrease in the width of the base region, so emitter current increases and base current decreases (I_E=I_B+I_C). **This effect is called early effect or based width modulation.**

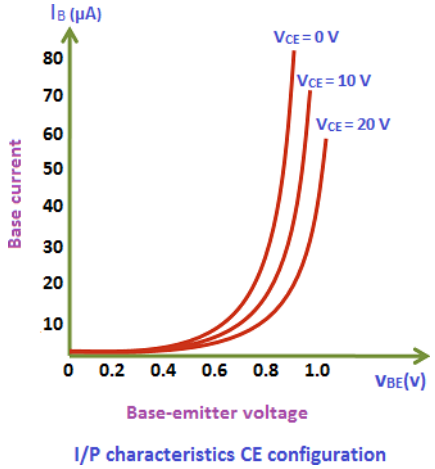


Figure 16: Input characteristics of CE configuration

Output characteristics

- V_{CE} vs I_C with zero or constant I_B
- If I_B is zero, and CB junction reverse-biased, a small current will flow through the device. This current is called reverse leakage current, denoted as I_{CEO}.
- $I_C = \beta I_B + (1+\beta) I_{CBO} - - - (1)$
- $I_C \approx \beta I_B - - - (2)$; β is the current amplification factor in CE configuration
- If I_B increases I_C also increases.
- **Effect of V_{CE}:** If V_{CE} increases base current decreases and collector current increases due to early effect.

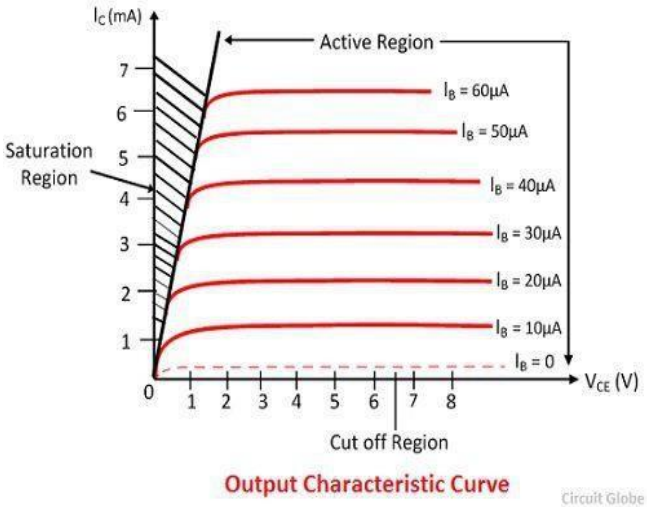


Figure 17: Output characteristics of CE configuration

Mathematical Expressions:

$$I_E = I_C + I_B - - - (1)$$
$$I_C = \alpha I_E + I_{CBO} - -(2)$$
$$I_C = \alpha(I_C + I_B) + I_{CBO}$$
$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$
$$(1-\alpha)I_C = \alpha I_B + I_{CBO}$$

Divide $(1-\alpha)$ *on both sides*

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{1}{(1-\alpha)} I_{CBO}$$
$$Let\ \beta = \frac{\alpha}{(1-\alpha)}; (1+\beta) = \frac{1}{(1-\alpha)}$$
$$I_C = \beta I_B + (1+\beta) I_{CBO}$$
$$I_C = \beta I_B + I_{CEO} - - - (3);$$

Where,

$$I_{CEO} = (1+\beta) I_{CBO}$$
$$Q = \frac{\boldsymbol{I_C}}{\boldsymbol{I_B}} = current\ gain\ or\ current\ amplification\ factor\ of\ CE$$

3. Common Collector (CC) Configuration

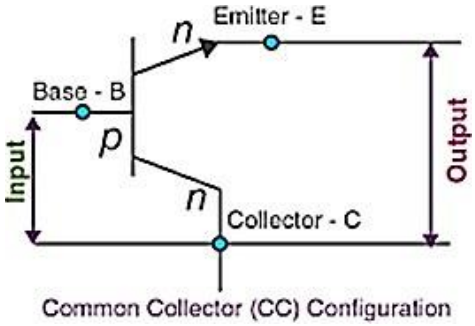


Figure 18: CC configuration

- Collector terminal is common (grounded) for both input and output
- Input is applied between B and C
- Output is taken across E and C
- I_B is the input current and I_E is the output current
- V_{BC} is the input voltage and V_{EC} is the output voltage

Where,

- I_B – Base current

- I_E – Emitter current
- V_{BC} – Base to Collector voltage
- V_{EC} - Emitter to collector voltage.

Figure () shows the circuit arrangement to obtain the VI Characteristics

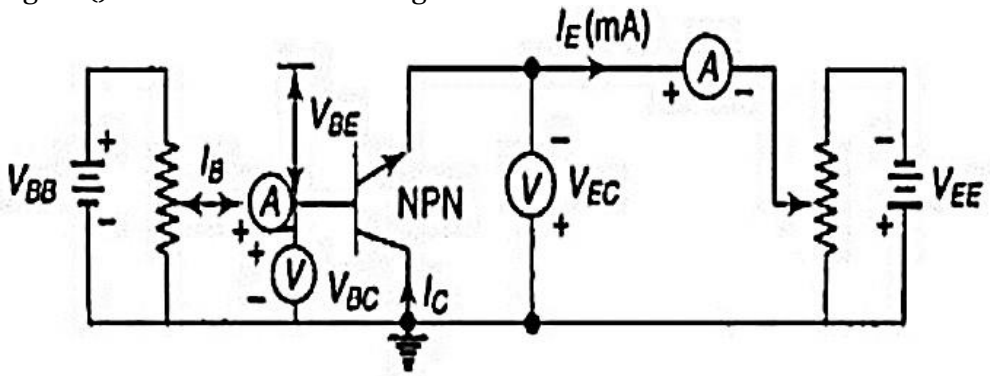


Figure 19: Circuit arrangement to obtain the VI characteristics

Input characteristics

- V_{BC} vs I_B with zero or constant V_{EC}
- Initially, the emitter to collector voltage V_{EC} is kept at zero.
- If VCB increases the CB junction depletion region increases and the width of the base region decreases, thereby decreasing the base current shown in figure.
- **Effect of V_{EC}:** If V_{EC} is increased, the depletion region of CB junction increases and depletion region penetrates deeper into the base region, which leads to further decrease in the width of the base region, so emitter current increases and base current further decreases.

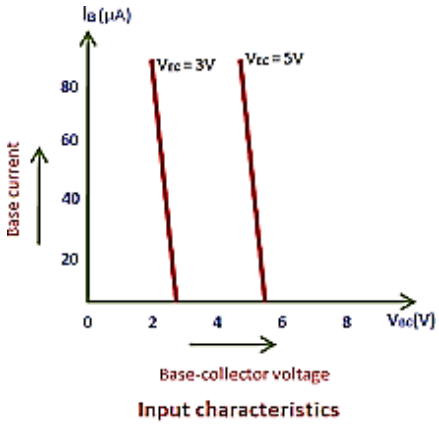


Figure 20: Input characteristics of CC configuration

Output characteristics

- V_{EC} vs I_E with zero or constant I_B
- If I_B is zero, and CB junction reverse-biased, a small current will flow through the device. This current is called reverse leakage current, denoted as I_{CBO}.
- $I_E = \gamma I_B + \gamma I_{CBO} \; --(1);$
  γ *is the current amplification factor in CC configuration.*
- The emitter current is proportional to the input current (Base current), the proportionality constant is the current amplification factor

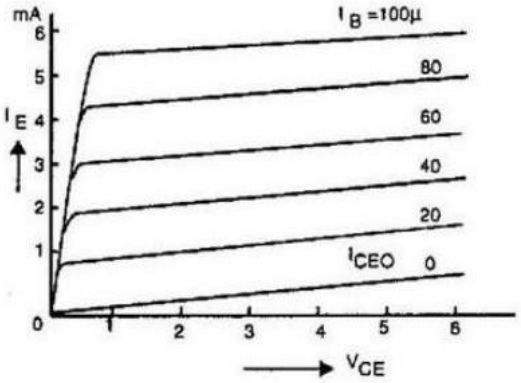


Figure 21: Output characteristics of CC configuration

Mathematical Expressions:

$$I_C = \alpha I_E + I_{CBO} - - - (1)$$
$$I_E = I_B + I_C - - - (2)$$
$$from,\ (2)$$
$$I_C = I_E - I_B - - - (3)$$
$$I_E - I_B = \alpha I_E + I_{CBO}$$
$$I_E - \alpha I_E = I_B + I_{CBO}$$
$$(1-\alpha) I_E = I_B + I_{CBO}$$
$$I_E = \frac{I_B}{(1-\alpha)} + \frac{I_{CBO}}{(1-\alpha)} - - - (4)$$
$$\text{Let, } \frac{1}{(1-\alpha)} = \gamma$$
$$I_E = \gamma I_B + \gamma I_{CBO}$$
$$I_E = \gamma I_B + I_{CCO} - - - (5)$$
$$I_{CCO} is\ the\ leakage\ current\ in\ CC\ configuration$$
$$I_{CCO} \ll \gamma I_B$$
$$I_E = \gamma I_B - - - (6)$$
$$= \frac{\boldsymbol{I_E}}{\boldsymbol{I_B}} \Rightarrow current\ amplification\ factor\ of\ CC\ configuration$$

Relation between a, Q ***and***

$$I_E = I_C + I_B - - - (1)$$

We know that, $\alpha = \frac{I_C}{I_E};\ \beta = \frac{I_C}{I_B}\ and\ \gamma = \frac{I_E}{I_B}$

Divide I_B on both sides

$$\frac{I_E}{I_B} = \frac{I_C}{I_B} + 1$$
$$= \mathrm{Q} + \mathbf{1}$$

Divide I_E, both sides

$$1 = \frac{I_C}{I_E} + \frac{I_B}{I_E}$$
$$1 = \alpha + \frac{1}{\gamma}$$
$$\alpha = 1 - \frac{1}{\gamma} \Rightarrow a = \frac{\mathbf{-1}}{\ }$$

Divide I_C, both sides

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C} \Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow\ a = \frac{\mathrm{Q}}{\mathbf{1} + \mathrm{Q}}$$

B in terms of α

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$
$$\frac{1}{\alpha} - 1 = \frac{1}{\beta}$$
$$\frac{1-\alpha}{\alpha} = \frac{1}{\beta}$$
$$\beta = \frac{\alpha}{1-\alpha}$$

Comparison of three configurations

Characteristic	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Shift	0^o	180^o	0^o
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

Transistor DC Load line analysis

Applying DC voltage of proper magnitude and polarity at the two junctions without AC signal is called DC biasing. When the BJT is biased, it will establish certain current and voltage conditions, these conditions are called operating conditions of the transistor.
In Common emitter configuration, collector to emitter voltage (VCE) and collector current(IC) are Operating conditions, these operating conditions are also called as DC operating point or quiescent point or simply Q-point. This operating point must be stable for the proper operation of the transistor.

Q point will be written in the following format: **Q (V_{CE}, I_C)**

In the following section, finding the Q point for CE configuration is explained.
Consider a BJT in common emitter configuration, Base-emitter junction is biased for the forward bias and Collector-base junction is biased for reverse bias. Resistors are connected through the base and collector terminals for biasing the device with proper magnitudes.

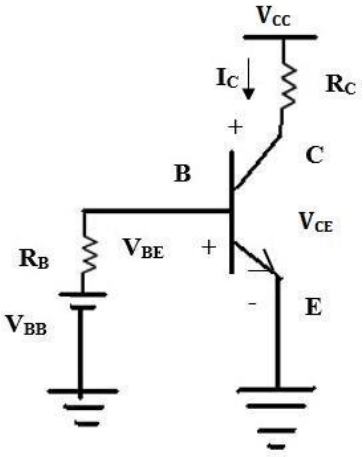


Figure 22: DC biasing of CE configuration NPN-BJT

The value of the collector current and emitter current at any time will satisfy

$$V_{CC} = I_C R_C + V_{CE} - - - (1)$$

If $V_{CE} = 0$,

$$\mathbf{I_{C(max)}} = \frac{\mathbf{V_{CC}}}{\mathbf{R_C}} - - - (\mathbf{2})$$

i.e., the collector current is maximum at zero collector-emitter voltage, denote this point as **A**.
If $I_C = 0$,

$$\mathbf{V_{CE(max)}} = \mathbf{V_{CC}} - - - (\mathbf{3})$$

i.e., the voltage across collector and emitter terminals is maximum, if collector current is zero, denote this point as **B**.

By locating the points A and B on output characteristics of common emitter configuration BJT, and joining the points gives DC load line. The intersection of the output characteristic curve and DC load line gives the operating point of the transistor. As shown in figure (23).

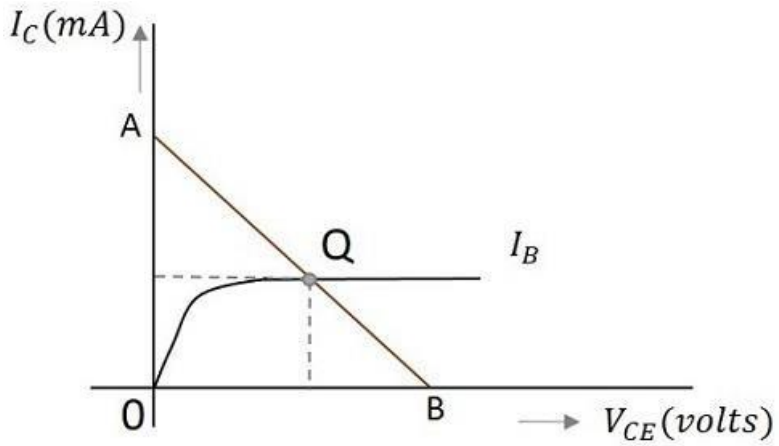


Figure 23: DC load line

The Q point must be at the middle of the active region for perfect amplification if the Q point moves towards the x-axis, the transistor will operate in cur-off mode and if the Q point moves towards the Y-axis, then the transistor will operate in saturation mode. The slope of the DC load line is $\frac{-1}{R_C}$.

NOTE:

1. The leakage current, I_{CBO} greatly affected by temperature variations. The collector to base leakage current doubles for every 10°C rise in temperature.

$$I_{CBO}at\ t_2 = I_{CBO}at\ t_1 * 2^{\frac{t_2-t_1}{10}} - - - (4)$$

Also,

$$I_{CEO} = (1+\beta)I_{CBO} - - - (5)$$

And,

$$I_{CCO} = \gamma I_{CBO} - - - (6)$$

Collector current depends on I_{CBO} which is the temperature-dependent quantity and hence, the Q point may shift towards saturation or cut-off region, leads to unexpected behavior and response from the system. This process is termed as a **thermal run-away**, i.e., destruction of Q point due to temperature variations is called thermal run-away. So, proper biasing is necessary to maintain the location of the Q point constantly.
Also, V_{BE} is a temperature-dependent variable, which decreases by 2.5mV for every 1°C rise in temperature.

2. The Q point also depends on the value of β, β is a highly sensitive factor, and small changes in the input current lead to very high changes at the output (Collector current and collector to emitter voltage). So, proper biasing is necessary to maintain the location of Q point constantly.
i.e.,

$$\Delta I_C = \beta \Delta I_B - - - (7)$$

3. Location of the Q point and its corresponding response.

i. If the Q point is at the middle of the active region

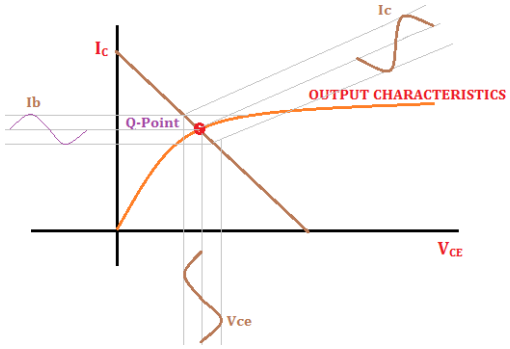


Figure 24: Q point is located in the middle of the active region.

ii. If the Q point is nearer to the cut-off region

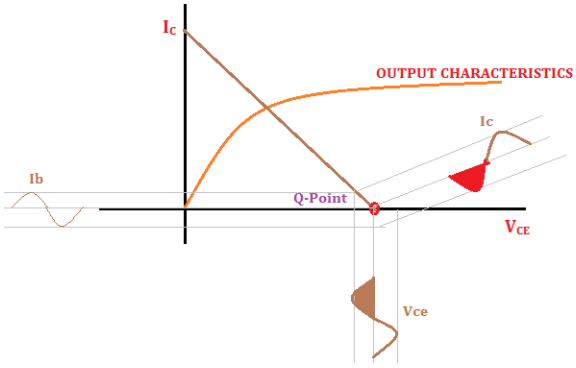


Figure 25: Q point is located the on x-axis

iii. If the Q point is nearer to the saturation region

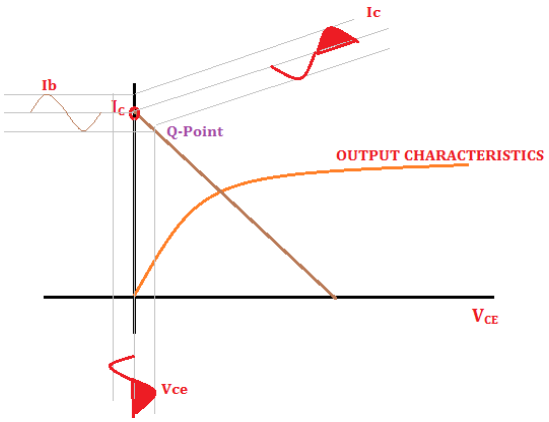


Figure 26: Q point is located the on y-axis

Transistor as an amplifier:

Amplifier is an electronic circuit, which increases the strength of the weak signal, in otherward amplifier is an electronic circuit, which increases the amplitude of the input (current or voltage or both) signal.

Common emitter configuration of BJT is best suitable for amplification purpose, because common collector configuration can amplify both voltage as wells as current.

Consider a common emitter configured BJT with simple biasing method, shown in figure (27). RB is the base resistor and RC is the collector resistor which is to be properly chosen to maintain the location of the Q point in the middle of the active region for zero signal.

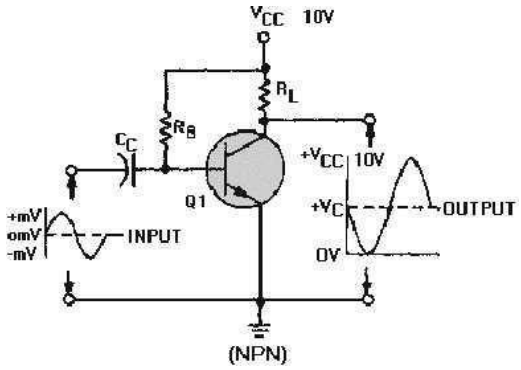


Figure 27: Transistor amplifier circuit.

When an ac signal is applied across the base to emitter terminal, that signal superimposed with the DC base current. The small change in base current ΔIb provides a very high change in collector currentΔI_c, because of largeβ.

i.e.,

$$\frac{\Delta I_b}{\Delta I_c} = \text{Q} - - - (\mathbf{1})$$

Current amplification

Assume, r_e is the internal emitter resistance of the PN junction (EB Junction) and

$$V_b = Ib_{RB} - - - (2)$$

The output voltage is measured across Rl.

$$V_c = I_c R_L - - - (3)$$

$$we\ know\ that, I_c \approx I_e$$

$$\frac{V_c}{V_b} = \frac{R_L}{R_B}\text{Q} - - - (\mathbf{4})$$

Voltage amplification

Transistor as a switch:

Figure shows the circuit arrangement to utilize the transistor as a switch. Collector terminal is biased with VCC through RC and base terminal is biased with V_{BB} through R_B. R_B and

R_C decides the transistor to work in saturation and cu-off region with respect to V_{BB}. The switching action of transistor is discussed as follows.

Case (i): Cut-off
If V_{BB}=0, based current is zero and hence collector current through the transistor is zero lead to collector to emitter voltage is equal to the applied voltage V_{CC}, hence the terminals collector and emitter acts as an open circuit called OFF switch.

$$\text{i.e., } V_{CE(saturation)} = V_{CC} - - - (1)$$

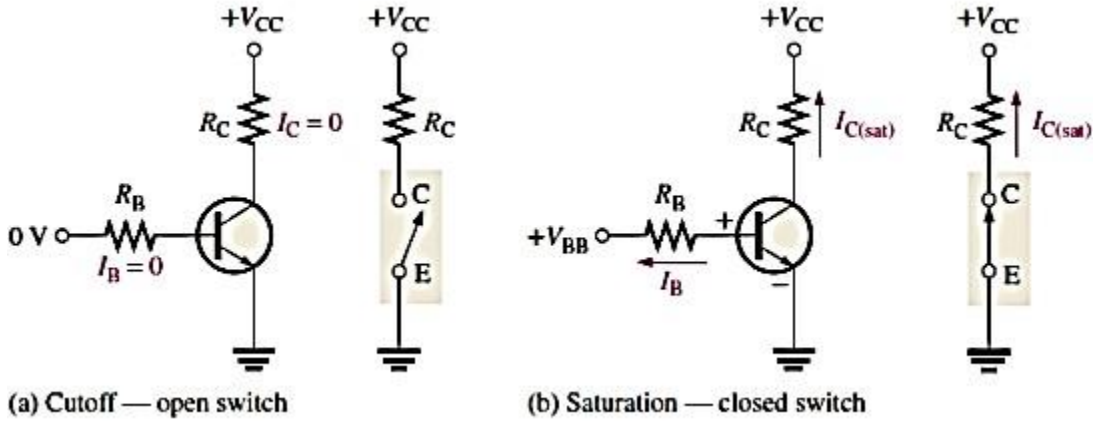


Figure 27: Transistor .

Case (ii): Saturation
When positive voltage of sufficient magnitude applied across the base terminal, base to emitter junction conducts and sufficient base current will drive the transistor to saturation region and maximum collector current flows through the device. Hence, the collector to emitter terminal acts as a short circuit and called ON switch.

$$i.e., I_C(saturation) = \frac{V_{CC} - V_{CE(saturation)}}{RC} - - - (2)$$

$$V_{CE}(saturation) = 0$$

$$I_{C(saturation)} = \frac{V_{CC}}{R_C} - - - (3)$$

Example to show the amplifier and switch action of transistor.

Consider $V_{CC} = 5V, R_C = 1K\Omega,\ \beta = 100$
We know that, $V_{CE} = V_{CC} - I_C R_C$

$$\text{If } I_B = 0, V_{CE} = V_{CC} => 5V\ (\textbf{cut} - \textbf{off})$$

If $I_B = 10\mu A, V_{CE} = 4V$
If $I_B = 20\mu A, V_{CE} = 3V$ } **(Active region)**
If $I_B = 30\mu A, V_{CE} = 2V$
If $I_B = 40\mu A, V_{CE} = 1V$

$$\text{If } I_B = 50\mu A, V_{CE} = 0V\ (\textbf{Saturation})$$

$$10 < I_B < 50\mu A => Active\ region$$
$$I_B > 50\mu A => switch$$

Design of RB to operate the transistor as an amplifier

$$I_B min = 10\mu A$$

$$I_B max = 50\mu A$$

Assume $V_{BB} = 5V$

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} - - - (1)$$

$$R_B min = \frac{5 - 0.7}{50\mu} => 86K\Omega$$

$$R_B max = \frac{5 - 0.7}{10\mu} => 430K\Omega$$

R_B should be choosen between 86 K to 430K

Design of RB to operate the transistor as a switch

If $V_{BB} = 0; I_B = 0, independent\ of\ R_B$ and $V_{CE} = V_{CC}$ $(cut - off)$

If $V_{BB} = 5V;\ for\ I_B > 50\mu A$

$R_B < 86K\Omega$

Verification:

$If\ R_B = 80K\Omega; I_B = 53.75\mu A, I_C = 5.375m$

$\boldsymbol{V_{CE} = V_{CC} - I_C R_C => 0 Volts (Saturation)}$

******

Feedback amplifier.

Feedback is a process/technique where a portion of the output signal of a system is **fed back** and **recombined** with the input.

- Feedback is used in all amplifier circuits.
- Some circuits virtually acts as a feedback in electronic systems and also can be introduced externally for some amplifiers.
- Invented in the year 1928 by Harold black, engineer, Western electric company.

Figure (1) shows the canonical form representation of a feedback system, block A_{OL} is the amplifier with gain A or A_{OL} and block β is the feedback network with gain β.

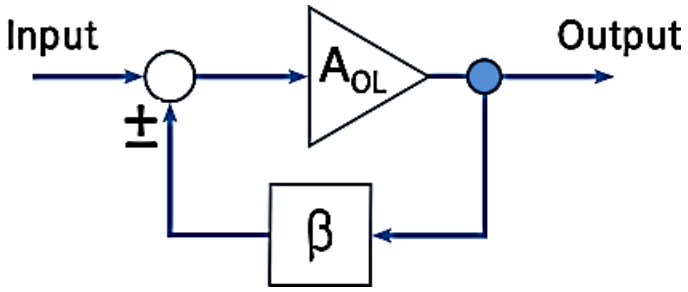


Figure 1: Canonical for representation of feedback system

Based on the way of combining the signals at input, feedback systems are classified into:

- Positive feedback
- Negative feedback

Positive Feedback:

- Positive feedback is a process of **adding** the portion of the output with the input and amplifying. This process is continuous and regenerative action takes place shown in figure (2).

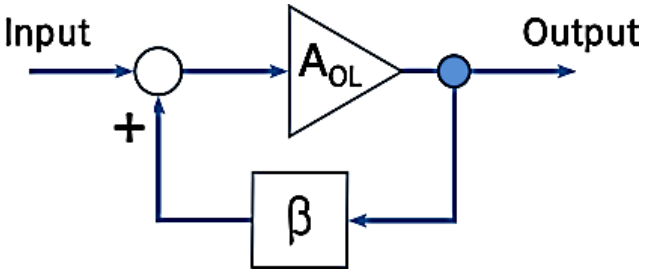


Figure 2: Canonical for representation of positive feedback system

Though the positive feedback **increases the gain** of the amplifier, it has the disadvantages such as

- Increasing distortion
- Instability

NOTE: Positive feedback is mainly used in the design of oscillators.

Negative Feedback:

- Negative feedback is a process of **subtracting** the portion of the output with the input and amplifying. This process is continuous and degenerative action takes place shown in figure (3).

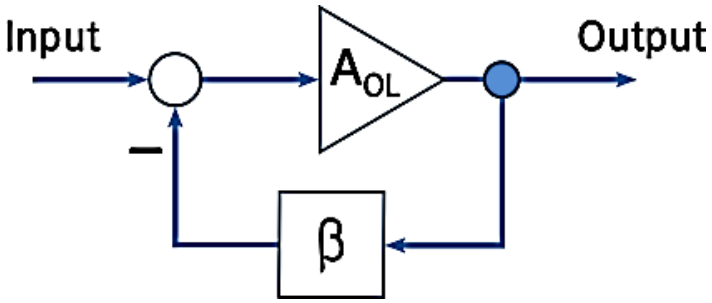


Figure 3: Canonical for representation of negative feedback system

NOTE: Negative feedback is used in the design of all types of amplifiers.

Advantages of Negative Feedback/Properties of negative feedback:

- Stabilizes the gain
- Increases the input impedance
- Decreases the output impedance
- Bandwidth increases
- Increases upper cut-off frequency
- Decreases the lower cut-off frequency
- Decreases the distortions
- Reduction in noise

Disadvantage:

- Decreases the gain

Basic structure of feedback amplifiers

Figure (4) shows the basic structure of a feedback system, which consisting of input unit, output unit, summing network, sampling network, basic amplifier and feedback network. The function each of these blocks are explained as follows.

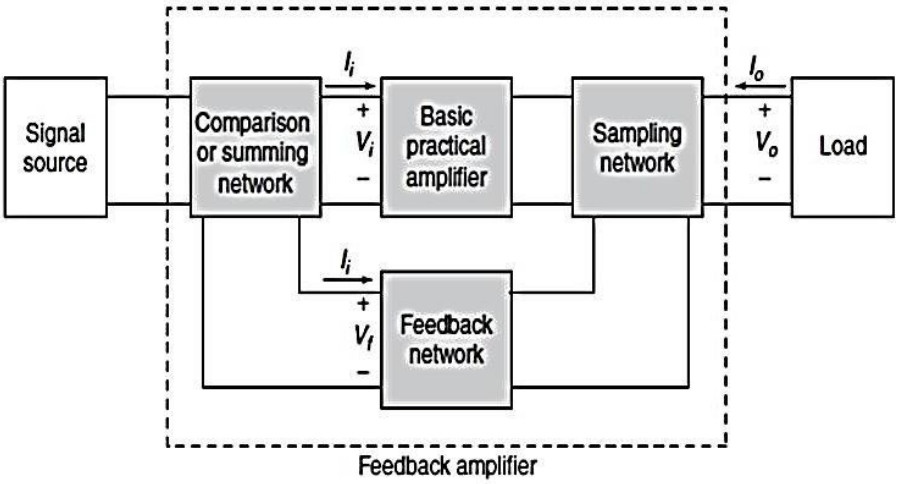
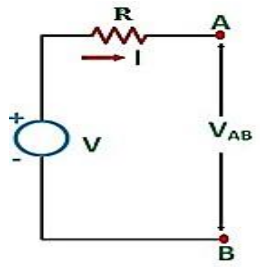


Figure 4: Basic block diagram of neagative feedback system

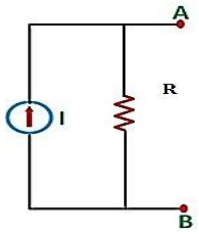
1. Input signal:

- It is a source wither modelled by a practical voltage source or practical current source.
- An ideal voltage source in series with a resistor is called practical voltage source
- An ideal current source in parallel with a resistor is called practical current source.

Practical voltage source



Practical Current source



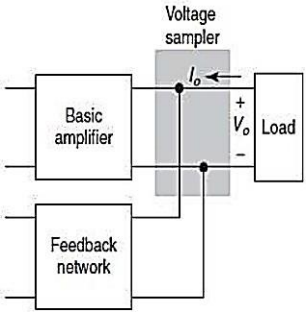
2. Output signal:

- The output of the system is either voltage across the load or current through the load.
- The output of the feedback amplifiers must be independent of the load variations and parameter variations in the amplifier.

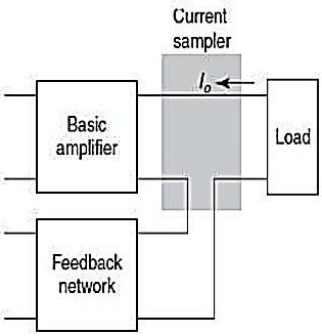
3. Sampling Network :

- A network is used to mesure and sending the output signal to the feedback network is called sampling network.
- For measuring the voltage a parallel(shunt) connection is required
- For measuring the current a series connection is required

Voltage measurement



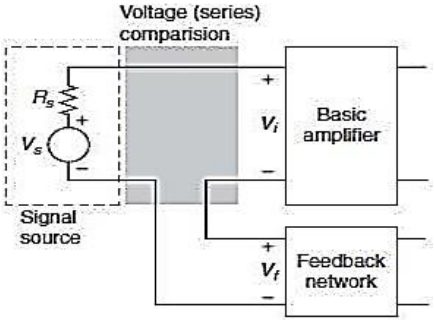
Current measuremen



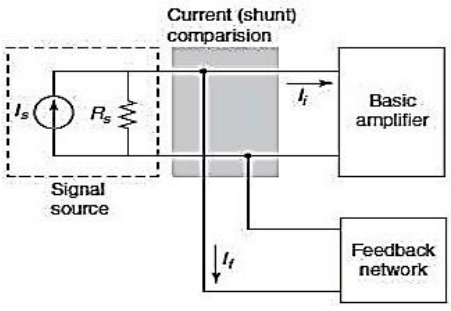
4. Comparison or summing network:

- Comparing the output signal with the input signal.
- Comparing voltage signals – series network
- Comparing the currents signals – parallel(Shunt) network

Voltage summing



Current summing



5. Amplifier:

- Amplifies the compared or combined signal
- Electronic circuits

6. Feedback network:

- Combination of electronic/electrical/both elements
- Provides the feedback signal in proportional to the output signal.

Based on the type of summing network and sampling network, feedback systems are classified into four types, they are.

1. Voltage - Series negative feedback
2. Voltage - Shunt negative feedback
3. Current - Series negative feedback and
4. Current - Shunt negative feedback

1. Voltage Series negative feedback

Summing network is a series network and sampling network is a shunt network, output voltage is fed to the feedback network and feedback voltage and input voltage are combined at the summing netwrk. Actual inpt to the amplifier circuit is the difference of the feedback voltage and supply voltage. Figure (5) shows the block diagram of voltage series negative feedback system.

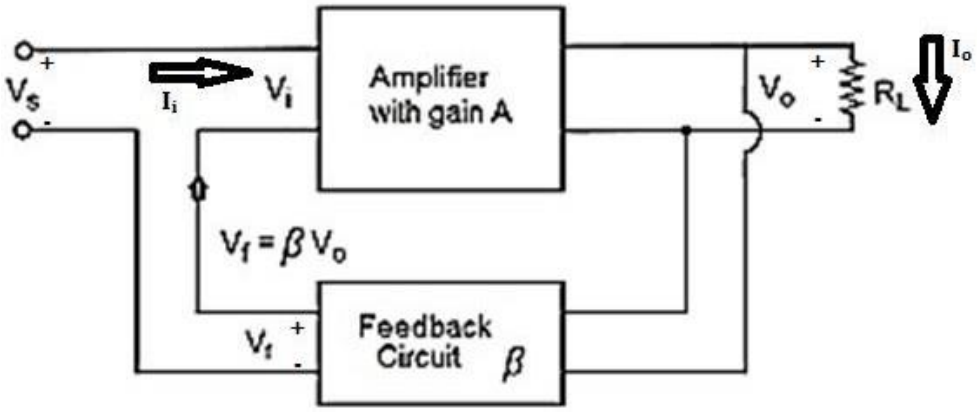


Figure 5: Block diagram of voltage series negative feedback system

Property-1: Reduces the overall gain and stabilizes the gain

Proof:

$$V_o = AV_i - - - (1)$$
$$V_i = V_s - V_f - - - (2)$$
$$V_f = \beta V_o - - - (3)$$
$$V_o = A[V_s - V_f]$$
$$V_o = A[V_s - \beta V_o]$$
$$V_o = A[V_s - \beta V_o]$$
$$V_o = AV_s - A\beta V_o$$
$$V_o[1 + A\beta] = AV_s$$
$$\frac{V_o}{V_s} = \frac{A}{1+AQ} - - - (4)$$ **Closed loop gain**

Example:

P1: If gain of the amplifier is 10^5, what is the overall gain after introducing the feedback with feedback gain 0.01? Also compare the overall gain if the gain of the amplifier is changed by ±50%

Given data:

$$A = 10^5 \; and \; \pm 50\%$$
$$\beta = 0.01$$

To find:

$$A_{CL} \; for \; A \; and \; A \pm 50\%$$

Solution:

$$A_{CL1} = \frac{A}{1 + A\beta} \Rightarrow \frac{10^5}{1 + 10^5 * 0.01} \Rightarrow 99.9$$
$$A_{CL2} = \frac{A + 50\%}{1 + A\beta} \Rightarrow \frac{150000}{1 + 150000 * 0.01} \Rightarrow 99.93$$
$$A_{CL3} = \frac{A - 50\%}{1 + A\beta} \Rightarrow \frac{50000}{1 + 50000 * 0.01} \Rightarrow 99.8$$

Property-2: Increases the input impedance

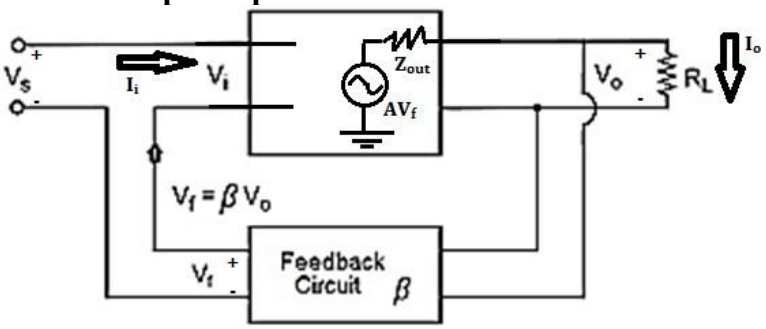
Proof:

$$Z_{in} = input \; impedance \; without \; feedback \Rightarrow \frac{V_i}{I_i}$$
$$Z_{if} = input \; impedance \; with \; feedback \Rightarrow \frac{V_s}{I_i}$$
$$Z_{if} = \frac{V_s}{I_i} \Rightarrow \frac{V_s}{\cancel{V_i}} * \frac{V_i}{\cancel{I_i}} \Rightarrow \boldsymbol{\frac{V_s}{V_i} * Z_{in}} - - - (\mathbf{1})$$
$$V_i = V_s - V_f$$
$$V_i = V_s - \beta V_o$$
$$V_i = V_s - \beta A V_i$$
$$V_i[1 + A\beta] = Vs$$
$$\frac{V_s}{V_i} = 1 + A\beta - - - (2)$$

Substitute (2) in (1) we get

$$\boldsymbol{Z_{if} = (1 + AQ)Z_{in}} - - - (\mathbf{3})$$

Property-3: Decreases the output impedance



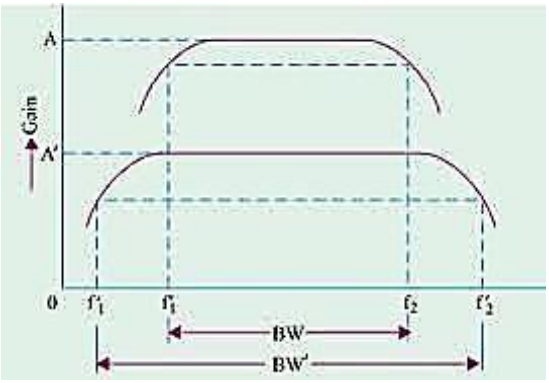
Proof:

$$Z_{out} = output \; impedance \; without \; feedback$$
$$Z_{of} = output \; impedance \; with \; feedback = \frac{V_o}{I_o}$$
$$AV_f + V_o = I_o Z_{out}$$
$$A[\beta]V_o + V_o = Z_{out} I_o$$

$$V_o[1 + A\beta] = I_o Z_{out}$$

$$\boldsymbol{Z_{of} = \frac{V_o}{I_o} \Rightarrow \frac{Z_{out}}{[1 + AQ]} - - - (1)}$$

Property-4: Bandwidth increases



$$\boldsymbol{BW = f2 - f1 - - - (1)}$$

$$\boldsymbol{BW_f = BW(1 + AQ) - - - (2)}$$

$$\boldsymbol{f_{1f} = \frac{f_1}{(1 + AQ)}}$$

$$\boldsymbol{f_{2f} = f_2(1 + AQ)}$$

Property-5: Reduction in distortion

$$\boldsymbol{Df = \frac{D}{(1 + AQ)}}$$

Property-6: Reduction in Noise

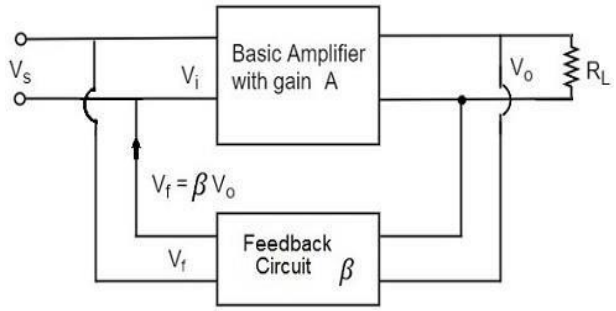
$$\boldsymbol{N_f = \frac{N}{(1 + AQ)}}$$

Summary:

Voltage Gain	Decreases and stabilizes
Bandwidth	Increases
Input resistance	Increases
Output resistance	Decreases
distortion	Decreases
Noise	Decreases

2. Voltage shunt negative feedback

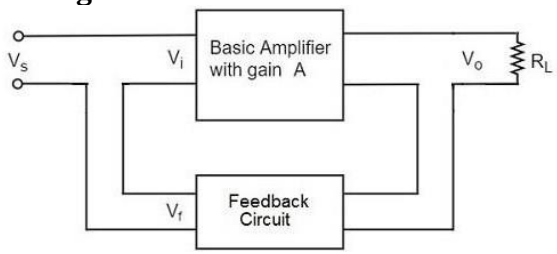
Block diagram



Properties	
Voltage Gain	Decreases and stabilizes the gain
Bandwidth	Increases
Input resistance	Decreases
Output	Decreases
distortion	Decreases
Noise	Decreases

3. Current series negative feedback

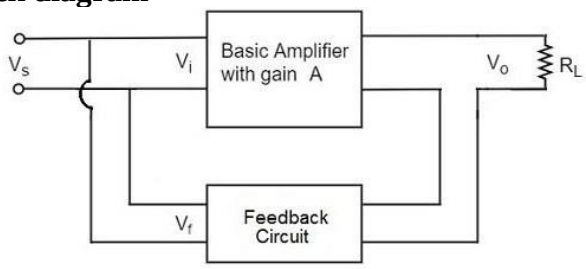
Block diagram



Properties	
Voltage Gain	Decreases and stabilizes the gain
Bandwidth	Increases
Input resistance	Increases
Output	Increases
distortion	Decreases
Noise	Decreases

5. Current shunt negative feedback system

Block diagram



Properties	
Voltage Gain	Decreases and stabilizes the gain
Bandwidth	Increases
Input resistance	Decreases
Output	Increases
distortion	Decreases
Noise	Decreases

By comparing the properties of all the four topologies of negative feedback systems, voltage series negative feedback has more advantages, and hence, voltage series negative feedback will be used for the design of amplifiers.

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Oscillators.

An Oscillator is an electronic circuit consisting of an amplifier with positive feedback, which generates the desired frequency of time-varying signals without an ac signal.

- Accepts DC and generates AC signals.

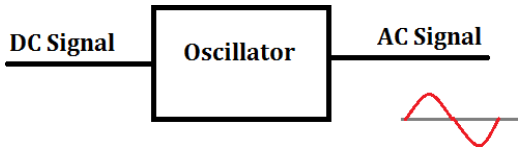


Figure 1: General operation of the oscillator

- Oscillators can generate the AC signal of frequency from few Hz to hundreds of GHz.
- An oscillator is an amplifier with positive feedback

Positive feedback and its closed-loop gain

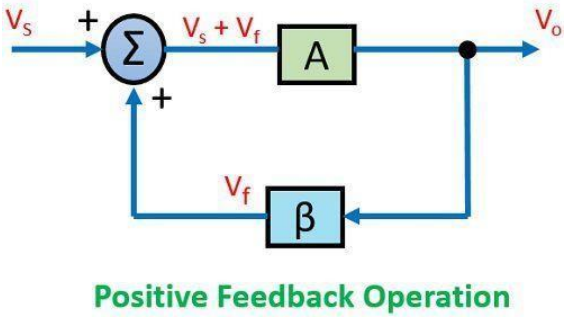


Figure 2: Canonical form representation of positive feedback system

Derivation of Closed Loop gain of the positive feedback system

$$V_o = A(V_i)$$
$$V_o = A(V_s + V_f)$$
$$V_o = A(V_s + \beta V_o$$
$$V_o = AV_s + A\beta V_o$$
$$\frac{\boldsymbol{V_o}}{\boldsymbol{V_s}} = \frac{\boldsymbol{A}}{\boldsymbol{1 - AQ}}$$

NOTE: The feedback signal is in phase with the input and hence, the feedback signal gets added with the input – **positive feedback**.

Effect of loop gain $\boldsymbol{A}$Q in the positive feedback system

Case (i): AQ > 1

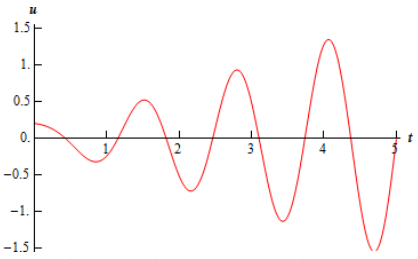


Figure 3: Output waveform of a positive feedback system, if Aβ > 1.

Case (ii): AQ < 1

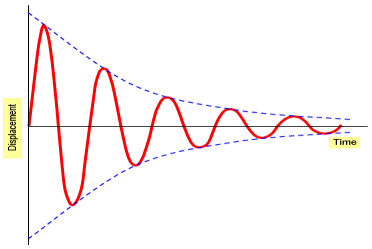


Figure 4: Output waveform a positive feedback system, if $A\beta < 1$.

Case (iii): $A\mathrm{Q} = \mathbf{1}$

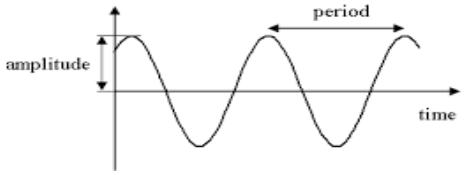


Figure 4: Output waveform a positive feedback system, if $A\beta = 1$.

Barkhausen's Criterion

Conditions to be satisfied for generation of sinusoidal Oscillations

Condition-1: The loop gain or Product of amplifier gain and feedback gain must be equal to one.

i.e., $|A\beta|=1$

Condition-2: Overall phase shift must be zero degree or 360 degrees

i.e., $\angle A\beta = 0^o$ **or** 360^o

Classification

Based on the output waveform

1. Sinusoidal
2. Non-sinusoidal

Based on the feedback circuit

1. RC Oscillators
2. LC Oscillators
3. Crystal Oscillators

Based on frequency

1. Audio frequency(20Hz to 20KHz)
2. Radiofrequency(20KHz-30MHz)
3. Very high frequency(30MHz to 300MHz)
4. UHF Oscillators (300MHz to 3GHz)
5. Microwave Frequency Oscillators(3GHz to 30GHz)
6. Millimeter-wave frequency oscillators (30GHz to 300GHz)

Based on electronic device/amplifier

1. BJT Oscillators
2. FET Oscillators
3. UJT Oscillators
4. Op-Amp Oscillators

1. RC phase shift oscillator

An oscillator is an amplifier with positive feedback.

- Amplifier circuit-CE configured BJT

- Feedback circuit – multiple stages of RC networks.
- Audio frequency oscillators – hundreds of KHz.

Circuit diagram

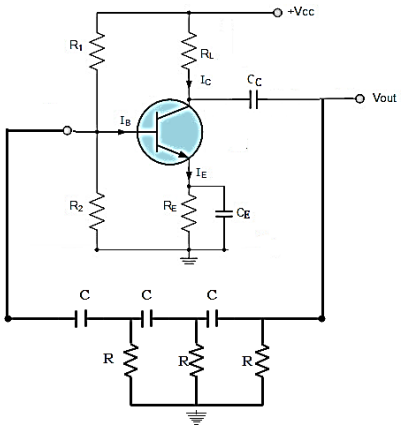


Figure 5: Circuit diagram of RC phase shift oscillator

Figure (5) shows the circuit diagram of the RC phase shift oscillator. BJT CE configuration is biased with voltage divider biasing technique using the resistors R_1 and R_2. R_C and R_E are collector and emitter resistors. C_C is a coupling capacitor that isolates the DC biasing settings and C_E is the bypass capacitor to avoid decreasing the output voltage by acting low resistance path across R_E under ac signal.

Further, three stages of the RC network are connected between the output terminal to the input terminal as a feedback circuit and this feedback circuit acts as a frequency selective network. Three stages of RC networks provide a constant attenuation factor of 1/29 (β) and an amplifier circuit should be designed to provide an amplification factor of 29(A), which satisfies the first condition of Barkhausen's criterion. Also, each RC stage is designed to provide a 60^o phase shift, so three stages of the RC network provide a 180^o phase shift and the BJT amplifier produces a 180^o phase shift. Hence, the total phase shift around a loop is 360^o or 0^o, which is the second condition of Barkhausen's criterion. Equation (1) is the expression of frequency of generated sinusoidal oscillations and figure (6) shows the waveform of generated oscillations.

The frequency of the generated sinusoidal signal is given by

$$\mathbf{f = \frac{1}{2\pi RC\sqrt{6}}}$$

Output waveform

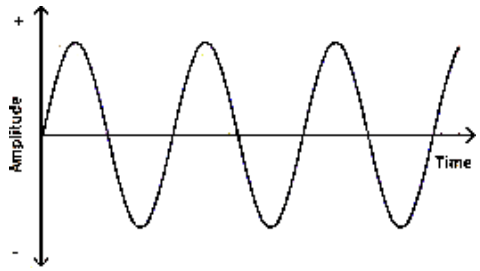


Figure 6: Output waveform of RC phase shift oscillator

LC oscillator basics.

- An oscillator is an amplifier with positive feedback.
- Amplifier circuit - CE configured BJT
- Feedback circuit – LC circuit (Tank circuit/resonant circuit/tuned circuit).

- Produces oscillations of up to 300KHz (Radio frequency)

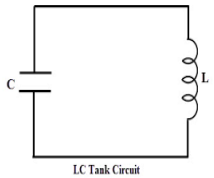
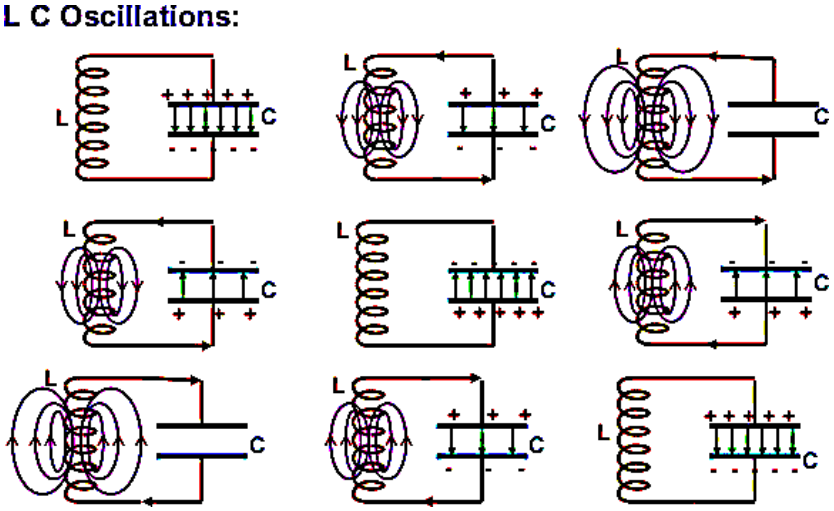


Figure 7: Tank circuit (LC circuit)

- The tank circuit is a Parallel connection of Capacitor and Inductor.
- Generates AC signal of frequency $f = \frac{1}{2\pi\sqrt{LC}}$
- Capacitor stores energy in the form of electrostatic field
- Inductor stores energy in the form of the electromagnetic field.
- Whenever a current flows through the inductor, a back e.m.f. will be established, which is the opposite polarity to the applied voltage.
- Energy stored across the elements is exchanged alternatively to produce an AC signal.

The following section is explained the working of the LC circuit to generate an AC signal.



1. Initially capacitor is charged to maximum level with the polarity shown

2. Capacitor starts discharging through the inductor and inductor starts charging.

3. Capacitor discharged completely and inductor charged to the maximum level

4. L starts discharging and C starts charging, due to back emf across the inductor

5. L discharged completely and C charged to the maximum level

6. Capacitor starts discharging through the inductor and inductor starts charging.

7. This process continuously takes place

There are two types of LC oscillators, they are Colpitts and Hartley oscillators. These two oscillators are discussed as follows.

2. Colpitts Oscillator

The Colpitts oscillator is an electronic circuit, which consisting of an amplifier circuit and an LC circuit as a feedback circuit shown in figure (8).

Circuit diagram

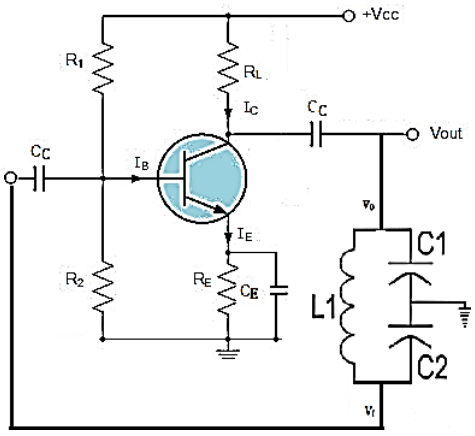


Figure 8: Circuit diagram of the Colpitts oscillator

Figure (8) shows the circuit diagram of the Colpitts oscillator. BJT CE configuration is biased with voltage divider biasing technique using the resistors R_1 and R_2. R_C and R_E are collector and emitter resistors. C_C is a coupling capacitor that isolates the DC biasing settings and C_E is the bypass capacitor to avoid decreasing the output voltage by acting low resistance path across R_E under ac signal. The feedback circuit is a series combination of two capacitors (C1, C2) across an inductor (L).

The amplifier gain is A and the feedback circuit gain β is $\frac{C1}{C2}$ by properly designing the circuits, Barkhausen's criterion condition number one can be achieved. i.e., $A\beta = 1$

The amplifier produces 180^o phase shift and the series connection of two capacitors provides phase inversion or 180^o phase shift, hence satisfies Barkhausen's criterion condition number two. i.e., $\angle A\beta = 0^o \; or \; 360^o$

Equation (1) is the expression of frequency of generated sinusoidal oscillations and figure (9) shows the waveform of generated oscillations.

The frequency of the generated sinusoidal signal is given by

$$\mathbf{f = \frac{1}{2\pi\sqrt{LC_{eq}}} \; C_{eq} - - - (1), \; where, \quad = \frac{C_1 C_2}{C_1 + C_2}}$$

Output waveform

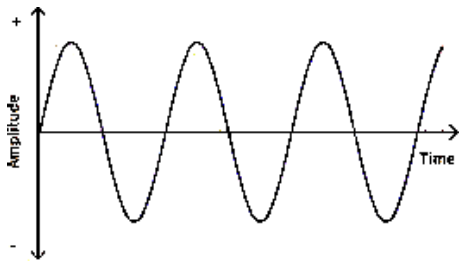


Figure 9: Output waveform of Colpitts oscillator

2. Hartley Oscillator

The Hartley oscillator is an electronic circuit, which consisting of an amplifier circuit and an LC circuit as a feedback circuit shown in figure (8).

Circuit diagram

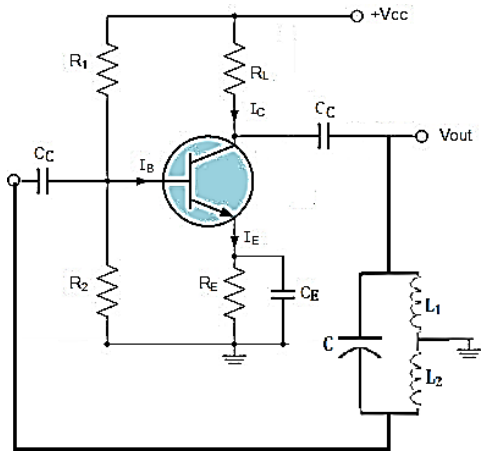


Figure 10: Circuit diagram of the Hartley oscillator

Figure (8) shows the circuit diagram of the Colpitts oscillator. BJT CE configuration is biased with voltage divider biasing technique using the resistors R_1 and R_2. R_C and R_E are collector and emitter resistors. C_C is a coupling capacitor that isolates the DC biasing settings and C_E is the bypass capacitor to avoid decreasing the output voltage by acting low resistance path across R_E under ac signal. The feedback circuit is a series combination of two Inductors (L1, L2) across a Capacitor(C).

The amplifier gain is A and the feedback circuit gain β is $\frac{L2}{L_1}$, By properly designing the circuits, Barkhausen's criterion condition number one can be achieved. i.e., $A\beta = 1$

The amplifier produces 180^o phase shift and the series connection of two inductors provides phase inversion or 180^o phase shift, hence satisfies Barkahusen's criterion condition number two. i.e., $\angle A\beta = 0^o \; or \; 360^o$

Equation (1) is the expression of frequency of generated sinusoidal oscillations and figure (11) shows the waveform of generated oscillations.

The frequency of the generated sinusoidal signal is given by

$$\mathbf{f = \frac{1}{2\pi\sqrt{L_{eq}C}} - - - (1), where, L_{eq} = L_1 + L_2 + 2M,}$$

where, M is the mutual inductance

Output waveform

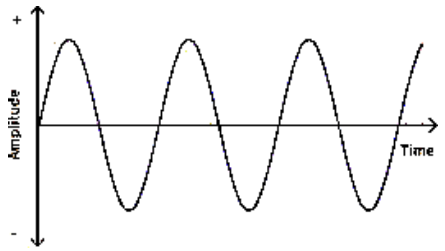


Figure 11: Output waveform of Hartley oscillator

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Field Effect Transistors(FETs) and Silicon Controlled Rectifier(SCR).

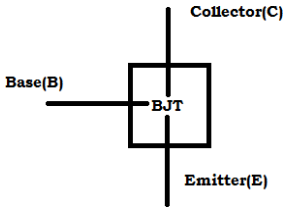
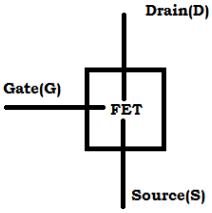
1. FETs:

FET is an acronym for the field-effect transistor. The FETs are three-terminal unipolar devices and conduction will be controlled by the electric field. Hence FETs are also called Field controlled/Voltage controlled devices.

Similarities between BJTs and FETs.

- Both are transistors.
- Both have two junctions and three terminals.
- Both are controlling the conduction of current and
- Both are semiconductor devices.

Difference between BJTs and FETs.

Sl. No.	BJTs	FETs
1		
2	Two Types • NPN(**N**ever **P**oints i**N**) • PNP(**P**oints i**N** **P**ermanently)	Two Types • N-Channel(points i**N**) • P-Channel(**P**oints out)
3	$I_C = f(I_B)$ i.e., $I_C = \beta I_B$	$I_D = f(V_{GS})$ i.e., $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
4	Collector Current is approximately equal to Emitter Current. $I_C \cong I_E$	Drain Current is equal to Source Current. $I_D = I_S$
5	Current Controlled Device	Voltage Controlled Device

6	Current conduction takes place by both holes and electrons. Hence Called Bipolar Transistors.	Current conduction takes place by only the majority charge carriers, either electrons or holes. Hence Called Unipolar Transistors.
7	Poor Thermal Stability	Good Thermal Stability
8	Low Input impedance	Very High input impedance
9	High Power Consumption	Low Power Consumption
10	Occupies More Space in a circuit	Occupies less space, hence can be fabricated easily in Integrated Chips.
11	**High Gain***	**Low Gain***
12	**Large Bandwidth***	**Bandwidth is low***

*Disadvantages of FETs over BJTs.

Classification of FETs.

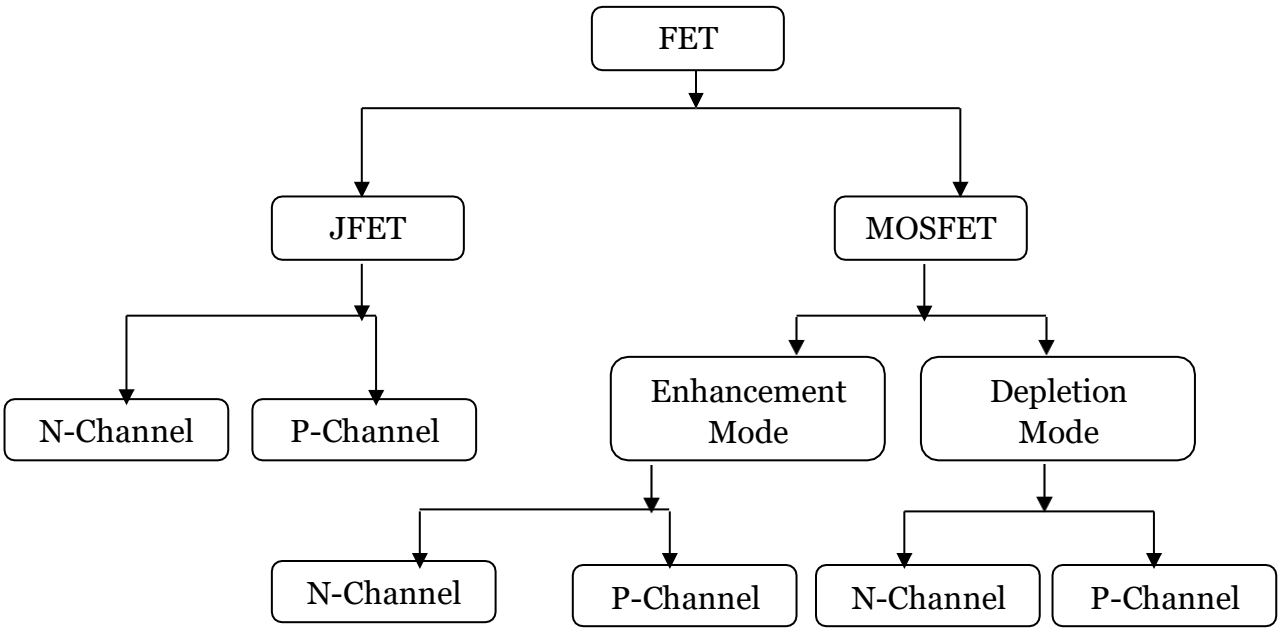


Figure 1.1: Classification of FET

N-channel and P-channel JFETs, Construction, Working principles, and Characteristics are discussed in the present context.

Analogy for discussing the working principle of JFETs:

A spigot/tap will be the best analogous system for JFET. Consider a tap shown in figure 1.6.

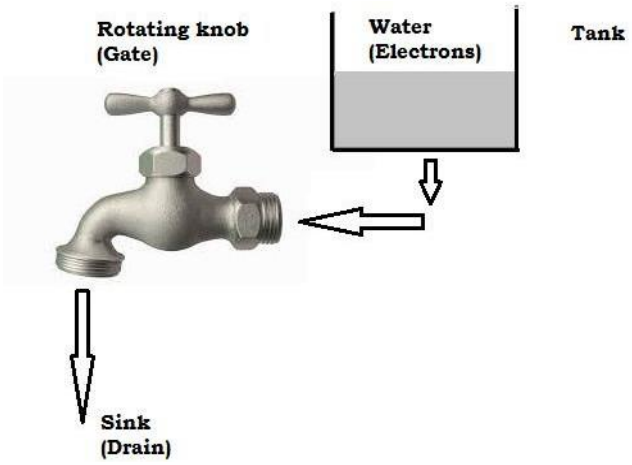


Figure 1.6. Analogous system for N-JFET.

Figure 1.6., shows a spigot/tap, in which the water will flow from the tank to the sink, and it will be controlled by rotating the controlling knob. Similarly in JFETs, the electrons will move from the source terminal to the drain terminal and will be controlled by the gate terminal. If the volume of the water in the tank is more, water movement will be faster, and more could be collected at the sink, similarly if the drain to source voltage increases, more electrons will drift from the source terminal to the drain terminal and causes a conventional current from drain to the source terminal, called as drain current.

Now consider a rotating knob of tap, that will be rotated to block the flow of water, but assume that it does not block completely. And due to more pressure of water flow from the tank, there should be a constant amount of water will flow. If the further increasing the pressure of water flow from the tank, the controlling element in a tap is going to damage, and more current will flow.

Similarly in JFET, if the pinch-off condition occurs, the constant current will flow from drain to source, which is due to the increase in drifting of electrons towards the drain terminal or due to high current density (conventional current will flow in opposite direction to the movement of the electrons). This occurs at $V_{DS}=V_P$ (Pinch-off Voltage). If $V_{DS}>|V_{VBD}|$, Junction will break and the device will get damaged.

N-Channel JFET.

In the N-channel Junction field-effect transistor, N-type material is the major part and the electrons are majority charge carriers, the current conduction takes place by these majority charge carriers.

Construction:

Starting with a large piece of N-type semiconductor material, it acts as a channel and two small pieces of P-type Semiconductor materials are embedded in the two sides of the N-type material, forming two PN Junctions shown in figure 1.2. The Major portion in the structure is the N-type semiconductor material and it is between the two P-type semiconductor materials that create an N-channel, hence called as N-Channel JFET.

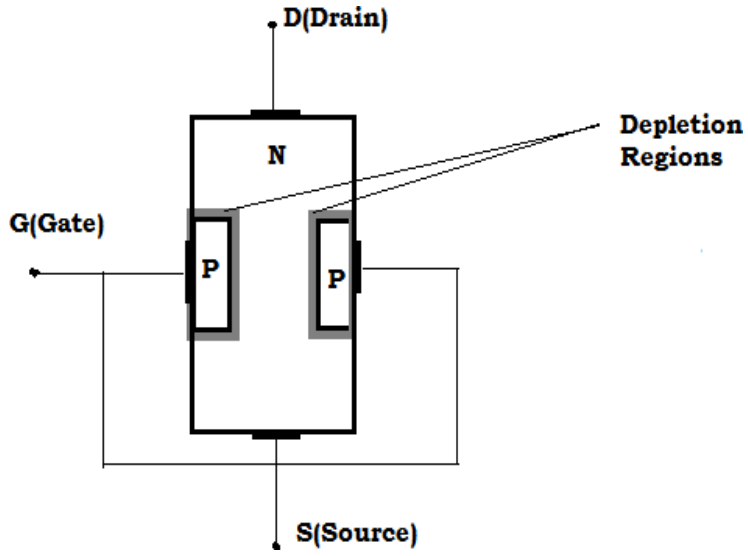


Figure 1.2: Structure of the N-Channel JFET.

The metallic contacts are deposited on the sides of the structure to connect the electrodes. The upper electrode is denoted as D and it is called as Drain terminal, the bottom electrode is denoted as S and it is called as Source terminal, the other two sides are internally connected and denoted as G and it is called as Gate terminal, shown in figure 1.2.

The N-Channel is having electrons that are majority charge carriers and holes are minority charge carriers, similarly, P-type materials are having holes that are majority charge carriers and electrons are minority charge carriers. Under normal room temperature, without bias, the electrons from the channel tend to move from N-type to P-type and vice-versa creates a small depletion region shown in figure 1.2.

Working Principle:

The working of N-Channel JFET will be discussed in two cases, as follows.

Case I: V_{GS}=0(Zero Gate Biasing) and V_{DS}>0V(Positive Voltage).

Case II: V_{GS}<0(Negative Biasing) and V_{DS}>0V(Positive Voltage).

Case I: VGS=0(Zero Gate Biasing) and VDS>0V(Positive Voltage).

The N-Channel JFET is Biased with a positive voltage between Drain to Source and Zero Biasing between Gate to source as shown in figure 1.3.

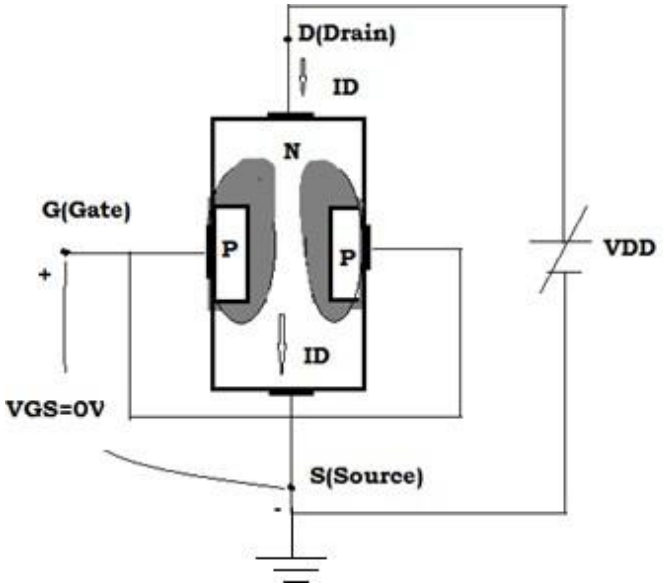


Figure 1.3. Under Positive Drain voltage and zero gate voltage.

By increasing the Positive voltage V_{DD}, the depletion region increases in the form of wedge shape shown in figure 1.3., because the PN Junction near the Drain terminal is reverse biasing and near the source terminal is forward biasing, hence the depletion region near the drain terminal is more compared to near the source terminal.

The shape of the depletion region is further explained in detail with the following analogy. The channel is like a resistor and considers there are five equal valued resistors are connected in series between drain to source shown in figure 1.4., suppose the applied voltage is 5 Volts, the voltage drop across each resistor is 1V.

With respect to A, the voltage is 1V, at B 2V, at C 3V, and at D 4V, i.e., the Positive voltage at D is more positive than C, at C is more Positive than B, and so on. Hence the width of the depletion region is more near the drain terminal compared to the Source.

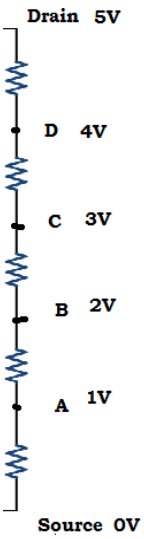


Figure 1.4. Showing Analogy for Channel.

If V_{DD} is increasing, the area and width of the channel decreases, hence less drain current will flow through the channel from drain to source, if V_{DD} is further increased to a level, which touches both the depletion regions(not overlapping) and it is called Pinch-Off. The voltage(positive voltage applied between drain to source) at which, the depletion regions are going to the Pinch-off condition, is called Pinch-off voltage shown in figure 1.5.

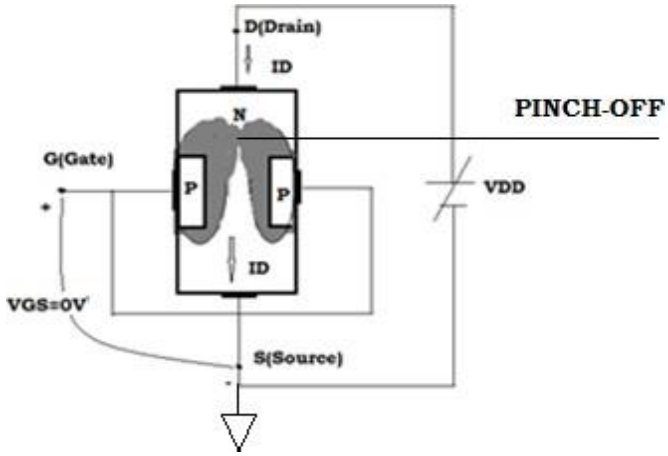


Figure 1.5. Pinch off condition

At Pinch-off condition, the constant current will flow from drain to source, because at pinch-off the depletion regions will touch but it will not create a barrier to move electrons from source to drain, and also due to high current density.

The output characteristic of N-Channel JFET is shown in figure 1.7.

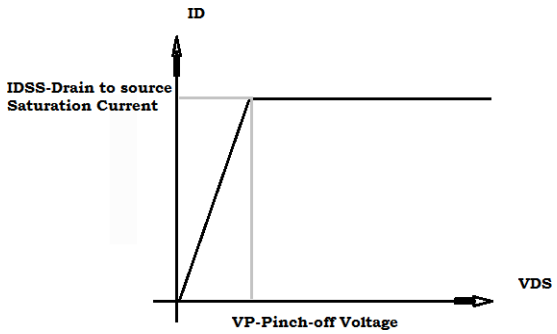


Figure 1.7. Output characteristics of N-channel JFET, with VGS=0 and VDS>0V.

Case II: VGS<0(Reverse Biasing) and VDS>0V (Positive Voltage).

The N-channel JFET's drain terminal is biased with positive voltage i.e. VDS=+ve, and the gate terminal is biased with negative voltage i.e., VGS=-Ve, shown in figure 1.8. In this case, the pinch-off condition occurs quite earlier and is decided by the negative potential applied at the gate i.e. more negative the V_{GS}, earlier the pinch-off, reducing I_{DSS} shown in the output characteristics, refer figure 1.9. As the phenomenon continues, it is seen that a condition arises wherein the saturation level of the drain-to-source current occurs right for a value of 0 mA. This means the current doesn't flow through the device and essentially the device will turn OFF. The value of V_{DS} for which this happens will be nothing but the negative pinch-off voltage i.e. $V_{DS} = -V_P$.

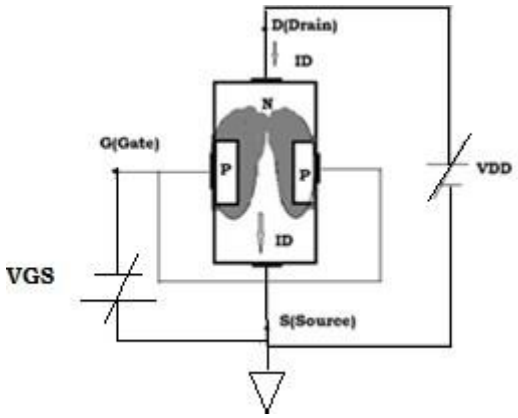


Figure 1.8: Forward biasing DS and Reverse biasing GS.

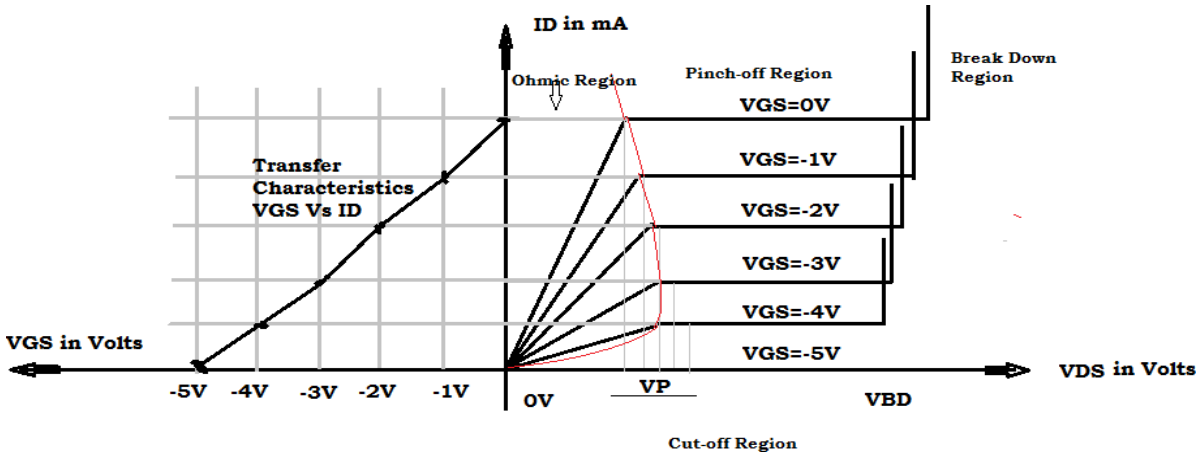


Figure 1.9: Drain and Transfer Characteristics of N-channel JFET.

Note: Students are informed to analyze the working principles of P-channel JFET.

2. SCRs:

SCR is an acronym for Silicon Controlled Rectifier.

- The device which converts ac to dc or the device which conducts current only in the forward direction is called rectifier/Diode.
- If the diode is made up of silicon material, then the diode is called a silicon diode/silicon rectifier. The silicon material is used instead of Germanium because of the requirement of high temperature to handle high currents and power.
- If the silicon diode is controllable, then the device is called a silicon-controlled diode/silicon-controlled rectifier.

Hence, the SCRs are defined as the devices which conduct current in the forward direction and also controllable and are made up of using silicon material. These devices have three junctions, three terminals, and four layers.

Basic Structure of SCR.

The basic Structure of SCR is shown in figure 2.1, which consisting of four layers, its four layers are arranged as PNPN. The outer layers are connected to terminals to form a positive terminal called an Anode, a Negative terminal called a Cathode, and a terminal from P-Layer nearer to the cathode called a Gate.

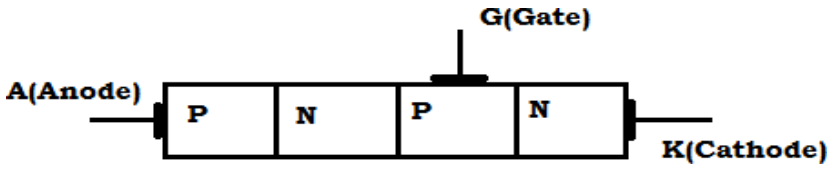


Figure 2.1: Basic Structure of the SCR

Circuit symbol.

The circuit symbol of SCR is shown in figure 2.2, the terminals anode, cathode, and gate are shown. I_A is Anode Current, I_G is the gate current, which is applying to control the anode current during the forward bias.

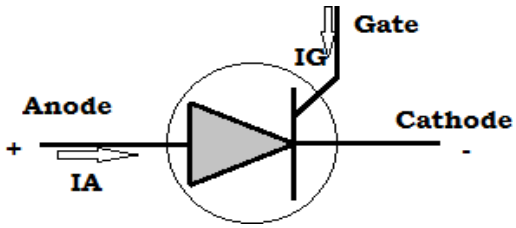


Figure 2.2: Circuit Symbol of SCR.

Working Principle.

Silicon Controlled Rectifiers begin their conduction during the forward bias, the forward biasing arrangement shown in figure 2.3. That is Positive terminal of the battery is connected to the anode terminal and the negative terminal of the battery is connected to the cathode terminal. The working principle of SCRs can be analyzed using two cases.

Case I: Without Gate signal(V_G=0 and V_{AA}>0).

Case II: With Gate signal(V_G>0 and V_{AA}>0).

Case I: Without gate signal(V_G=0) and V_{AA}>0.

When the SCR is under forward biasing and without the gate signal, as shown in figure The junctions J_1 and J_3 are forward biased and J_2 is reverse biased. Hence conduction path does not exist. During this condition, the device acts as an open circuit even under forward biasing.

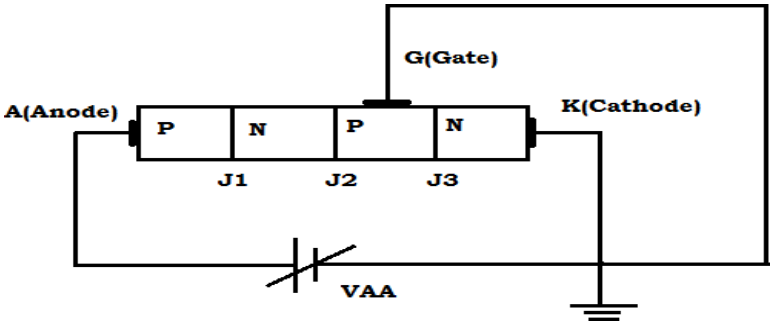


Figure 2.3: Forward Biasing of SCR without Gate Signal.

Case II: With Gate signal(V_G>0) and V_{AA}>0.

When a gate signal(Generally positive Clock Pulse) is applied along with forward biasing of SCR shown in figure 2.4. The gate current I_G(sufficiently large enough to drive the device) flows into the gate terminal and hence the junction J_2 gets forward biased along with J_1 and J_2, then the device goes to conduction mode and the current will flow from anode to cathode terminal. During this condition, the device acts as a short circuit/ON switch.

The silicon-controlled rectifiers, forward current offers a very low resistance of 0.01 to 0.1Ω, whereas it offers infinite resistance under non-conduction mode.

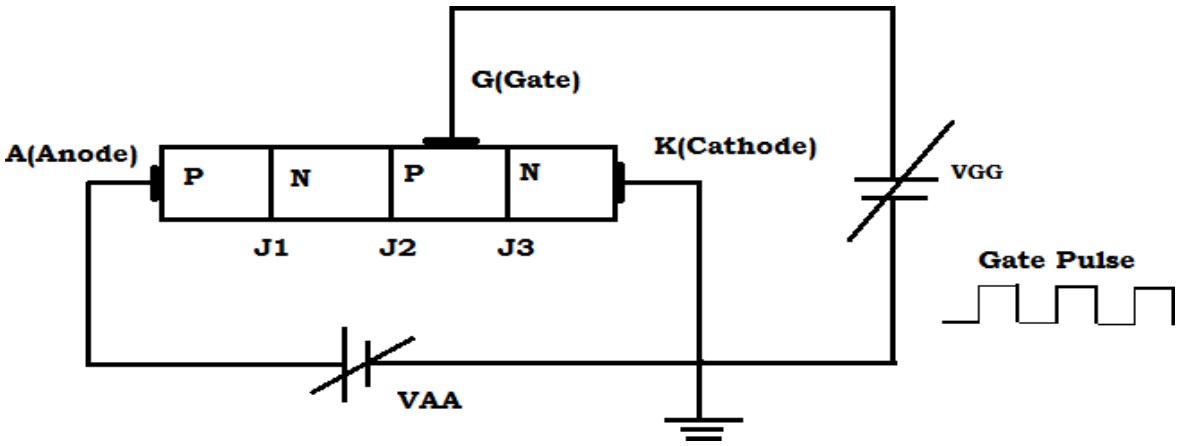


Figure 2.4: Forward Biasing of SCR with Gate Signal.

During forward biasing and with gate signal, all the junctions J_1, J_2, and J_3 are forward biased and regenerative action takes place. Because of regenerative action, even after removing the gate current, the device will not be turned off. Hence, an External circuitry/Commutation process is used to turn off the SCRs.

Two Transistor model or Analogy of SCR.

The two-transistor model of SCR is shown in figure 2.5. The four layers of SCR are divided into two transistors by subdividing the middle N and P Layers. The cross-sectional view of SCR is shown in figure 2.5(a) and the equivalent circuit using BJT symbols is shown in figure 2.5(b).

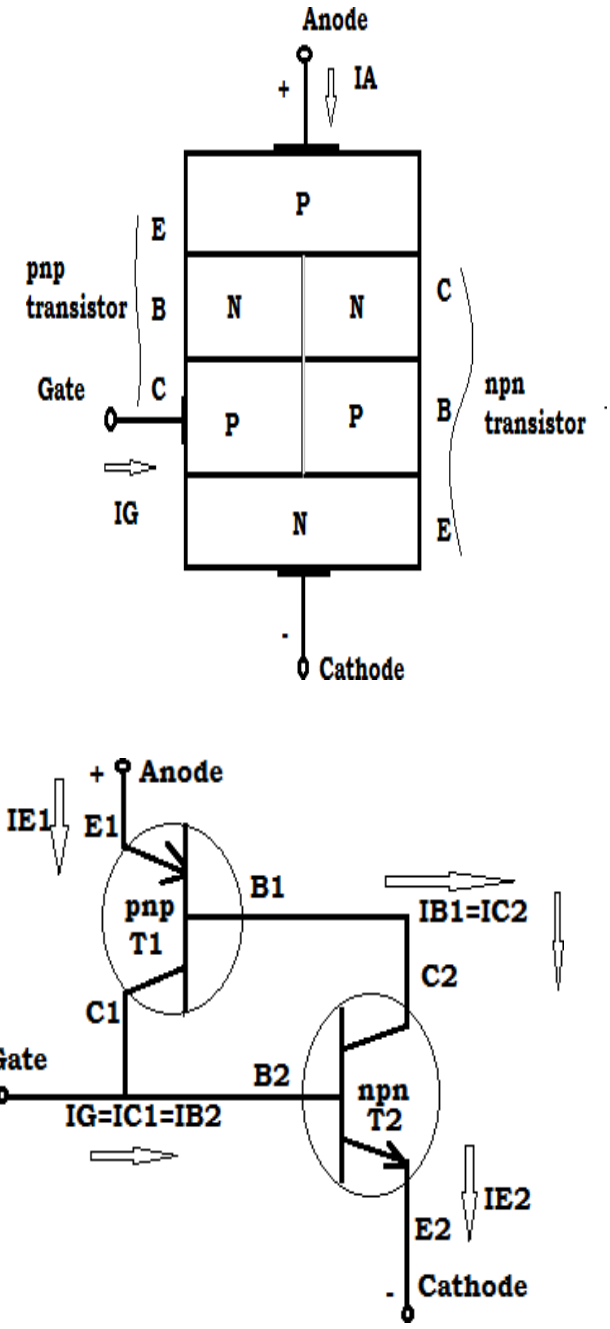


Figure 2.5(a): Cross sectional view. Figure 2.5(b): Transistor equivalent circuit.

Figure 2.5: Two Transistor model of SCR.

From the above diagrams, it is observed that the four layers of SCR are comprised of two transistors, one NPN and another PNP. As there is electrical continuity between the two

transistors, the base of the T_1 is connected to the Collector of T_2; and the collector of T_1 is connected to the base of T_2 is shown in figure 2.5b.

Switching action

Case-I: Without gate signal(V_G=0) and V_{AA}>0.

Gate(C_1/B_2) and Cathode(E_2) are connected to the ground terminal, i.e., the zero gate bias. Let a positive voltage V_{AA} be applied to the anode(E1). With V_G=0, the V_{BE2}=0 so, the CB junction of T_2 is reverse biased, and only leakage current(I_{CO}) will be supplied to the base of T_1. It is too small to turn on the transistor T_1. Thus both T1and T_2 are in the off state. Refer to figure 2.6.

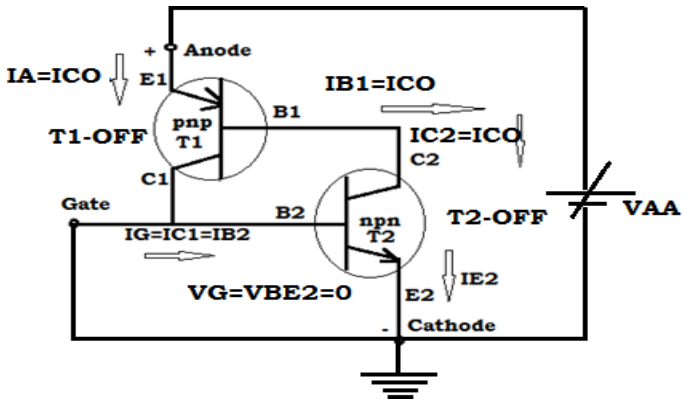


Figure 2.6: Showing Working principle of SCR under VG=0.

so anode current is given by, $I_A=I_{B1}=I_{CO}$ is of negligible quantity. That is SCR is in the turn-off state. means SCR acts as an Open Circuit or Open Switch.

Case-II: With Gate signal(V_G>0) and V_{AA}>0.

Let a Positive voltage V_G be applied at the gate terminal(C_1/B_2). As $V_{BE2}=V_G$, and on making V_G sufficiently large, I_{B2} will cause T_2 to turn on and the collector current I_{C2} becomes large. As $I_{B1}=I_{C2}$, T_1 turns on causing a large collector current $I_{C1}(I_A=I_{C1})$ to flow. This in turn increases I_{B2} causing a regenerative action to set in (this is indeed positive internal feedback). Refer to figure 2.7.

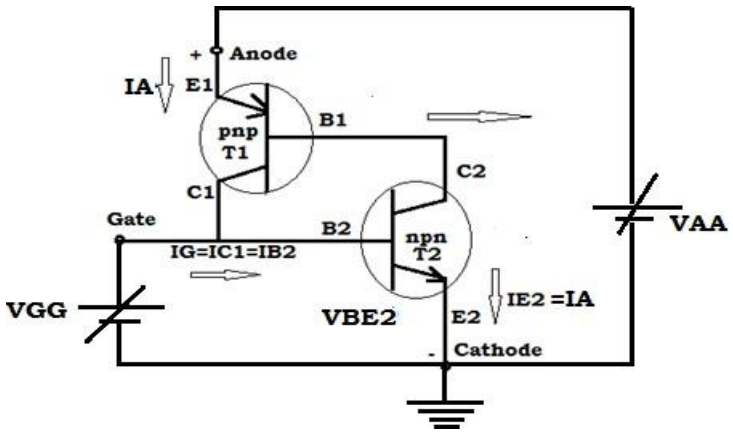


Figure 2.7: Showing Working principle of SCR under VG>0.

so anode current is given by, $I_A=I_{E1}=I_{E2}$ is of maximum current. that is SCR is led to turn-on. i.e., SCR acts as a short circuit or closed switch.

Commutation.

As observed from the switching action of SCR, once the SCR is turned on, due to regenerative action, the SCR always remains in ON condition, thus Commutation circuits/mechanisms are required to turn off the SCR.

Commutation is a process of turn-off the SCR, there are two types of commutation

- Natural Commutation
- Forced Commutation.

Natural Commutation.

The AC signal is fed to the SCR, when the signal passes through zero shown in figure 2.8, the current becomes zero, in that situation the SCR turns off naturally. This type of turning off the SCR is called natural commutation and also called line commutation.

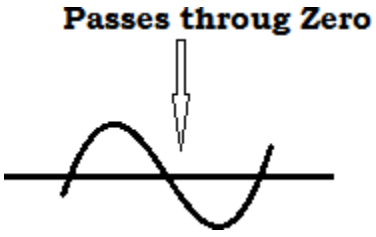


Figure 2.8: Signal Passes through Zero.

Forced Commutation.

Forced commutation is a process of turn-off the SCR, through an external circuit. In this case, the current through the SCR is forced to become zero by passing a current through it in opposite direction from the external circuit.

There are many types of forced commutation, in the present context, a simple series combination of the transistor and a dc battery is discussed to turn off the SCR as shown in figure 2.9.

To turn off the SCR, a positive I_B pulse of magnitude, large enough to drive the transistor into the saturation level is applied at the transistor base. the transistor acts as a short circuit. This causes the flow of very large I_{off} through the SCR in opposite direction to its conduction current. The total SCR current reduces to zero in a very short time causing SCR to turn off.

Turn off time of an SCR is typically 5-30μs.

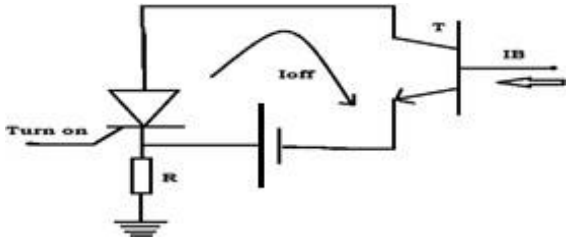


Figure 2.9: Turn-off Circuit

SCR Characteristics.

when the positive voltage $V_{AK}=V_F$ is applied between Anode to the cathode. Without a gate signal, a small leakage current will flow from anode to cathode due to minority charge carriers, which is negligibly small and considered as an OFF state. The voltage drop across the SCR is the same as the applied voltage, during the OFF state.

When a gate pulse is applied, the SCR will turn on, once the SCR turns on the voltage across the SCR i.e., V_{AK} drops to the threshold voltage level(Vt=0.7V, because Silicon controlled rectifier) and current suddenly increases. Further increase in V_F causes an increase in I_A but Voltage remains constant. The Plot of V_{AK} vs I_A is shown in figure 2.10 for different values of I_G.

If the forward break-over voltage V_F is small, more gate current is required to trigger the SCR.

The SCRs will trigger even without a gate signal if the voltage across the SCR exceeds V_{BD}(Break down voltage, practically very high voltage level).

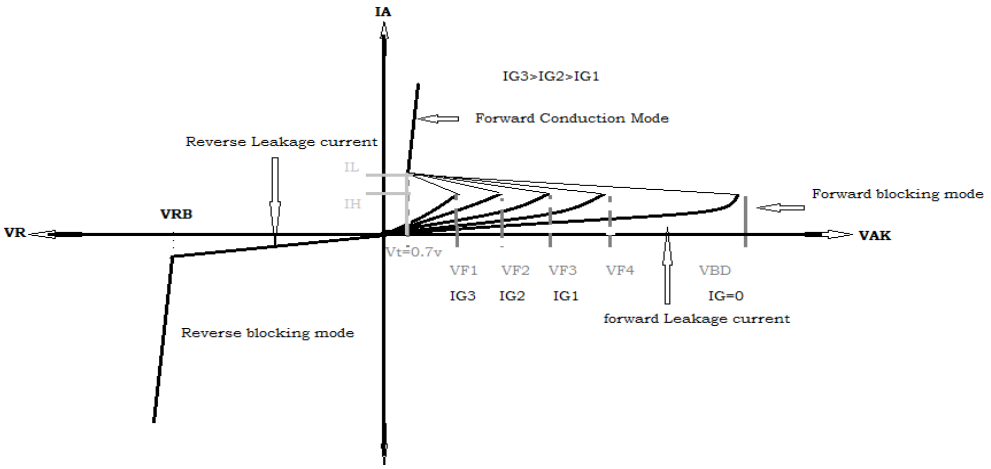


Figure 2.10: VI Characteristics of SCR.

Terminologies used in SCR and its characteristics.

a. Forward break-over voltage(VF)

Forward break-over voltage is the voltage at which for a given IG, the SCR enters into conduction mode. This voltage reduces as I_G increases.

b. Holding Current(IH)

Holding current is the value of the current below which SCR switches from conduction mode to forward blocking mode(OFF mode).

c. Forward and Reverse blocking

Forward and Reverse blocking regions are those regions in which the SCR is open-circuited and no current flows from anode to cathode.

d. Latching current(IL)

Latching current is the minimum anode current above which gate losses its control.

Operational Amplifiers and Digital Electronics.

Introduction

The operational amplifier in short Op-Amp is a linear Integrated circuit, also called a differential amplifier. Op-Amp is a linear and active device, which performs various operations like, signal conditioning, filtering, addition, subtraction, integration, differentiation, etc...

Op-amps are voltage amplifiers designed to be used with feedback circuits, using the elements Resistors or capacitors. The feedback elements determine the operation of the op-amps.

Op-Amps have three terminals, two input terminals named Inverting input terminal, Non-Inverting input terminal, and one output terminal. The op-Amp performs the amplification of the difference of the two input signals through +VCC and -VEE DC biasing power supply. Hence the name differential amplifier, shown in figure(1).

Circuit Symbol of an Op-Amp:

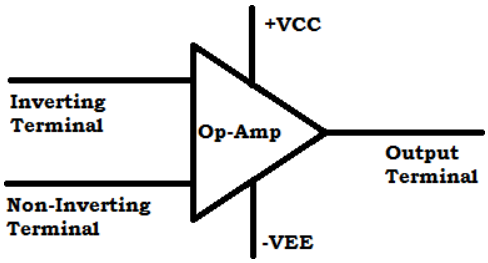
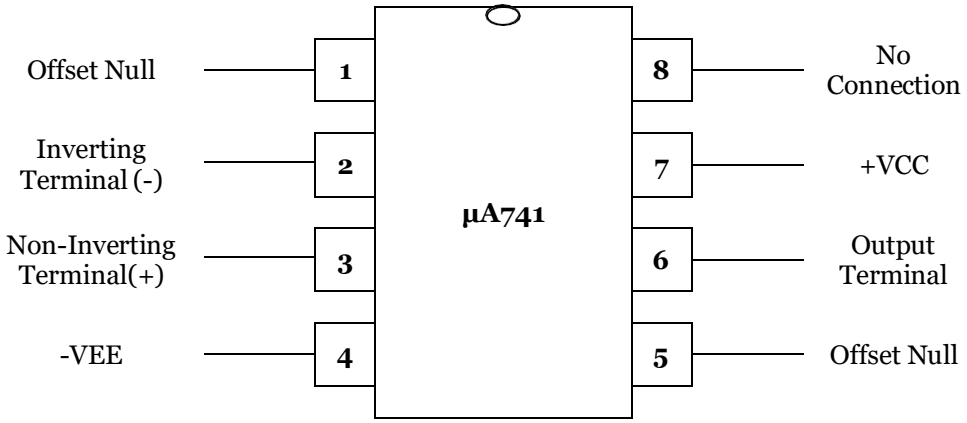


Figure 1: Circuit Symbol of an Op-Amp.

Op-amps come with an Integrated circuit(IC) package, which is an eight-pin IC, IC number is µA741.

Pin Details of µA741:

Figure(2) shows the pin diagram of IC µA741.



PINs 1 and 5 are offset null terminals, used to calibrate the op-Amp. Pin 2 is inverting input terminal, pin 3 is the non-inverting terminals, pin 6 is the output terminal, pin 4 and 7 are power supply terminals -VEE and +VCC respectively, and Pin 8 is no connection(NC) reserved for future enhancement.

Ideal Characteristics of Op-Amp:

i) Infinite Voltage Gain/loop gain

Voltage gain is the ratio of output voltage to the input voltage.

$$\text{i.e., } A_v = \frac{V_{out}}{V_{in}}$$

NOTE: Ideally ∞, typically $2x10^5$.

ii) Infinite input impedance

Input impedance is the ratio of input voltage to the input current, an Op-amp, the input current is zero., Hence, the Input impedance is infinite.

$$\text{i.e., } Z_i = \frac{V_{in}}{I_{in}}$$

NOTE: Ideally ∞, typically 1MΩ-2 MΩ.

iii) Zero output Impedance

Output impedance is the ratio of output voltage to the output current, in op-amp output current is maximum. Hence, the output impedance is zero.

$$\text{i.e., } Z_o = \frac{V_{out}}{I_{out}}$$

NOTE: Ideally 0, typically 50-75 Ω.

iv) Infinite Bandwidth

An op-amp has an infinite frequency response and can amplify the signal from DC to the highest frequencies.

NOTE: Ideally ∞, typically few GHz.

v) Infinite Common Mode Rejection Ratio(CMRR)

CMRR is the ratio of differential gain to the common-mode gain., Common-mode gain is the difference of the two input signals is zero. If Common mode voltage gain is zero, the CMRR is infinite.

$$\text{i.e., CMRR} = \frac{A_D}{A_{CM}}$$

$$A_{CM} = V_{inv} - V_{non-inv} \approx 0$$

NOTE: Ideally ∞, typically 70-90dB.

vi) Zero Slew rate

Slew rate is the rate of change of output voltage, which tells how fast the system responds to the change in the input signal.

$$\text{i.e., Slew Rate} = \frac{dV_{out}}{dt}$$

NOTE: Ideally 0, typically 0.5V/μsecs.

vii) Infinite Power supply rejection ratio(PSRR)

The ratio of change in output voltage to change in supply voltage(due to ac ripples) is called the Power supply rejection ratio.

$$\text{i.e, PSRR} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

NOTE: Ideally ∞,, typically 50-100dB

viii) Input Bias Currents:

The current flowing through the base terminals of the input stage transistors circuit of an op-amp is called input bias currents, denoted as I_{B1} and I_{B2}.

NOTE: Ideally 0A, typically 80nA and maximum 500nA.

ix) Input offset current:

The magnitude of the difference between the input bias currents is called Input offset current, denoted as I_{io}.

$$\text{i.e., } I_{io} = |I_{B2} - I_{B1}|$$

NOTE: Ideally 0A, typically 20nA, and maximum 200nA.

x) Input offset voltage:

Op-amp produces zero output voltage for zero input voltage, but practically a small dc voltage appears across the output terminal of an op-amp even if the input is zero, that voltage is called input offset voltage, denoted as V_{io}.

NOTE: Ideally 0V, typically 1mV, and maximum 5mV.

NOTE: The typical values given in the above characteristics are related to μA741.

Concept of Virtual ground

Op-amp is a differential amplifier, which amplifies the difference between the two input signals.

$$\text{i.e., } V_{out} = A(V_2 - V_1)$$

We know that, the ideally A=∞.

$$\text{Therefore, } V_{non-inv} - V_{inv} = 0$$

or

$$V_{non-inv} = V_{inv}$$

From the above equation, observed that the inverting terminal voltage is the same as the non-inverting terminal voltage. i.e., if one of the input terminals is connected to ground(zero potential), the other terminal voltage is also zero, which indicates that there are virtually short-circuited. In other words, a node that has zero potential with respect to the ground but is not connected to the ground. This concept is called virtual ground.

Applications of Op-amps

In this section, the linear applications of op-amp have been discussed.

Inverting amplifier

An electronic circuit or device, which increases the strength of the input signal and the output signal is 180° out phase with the input signal is called inverting amplifier. Figure(3) shows the circuit diagram of the op-amp inverting amplifier.

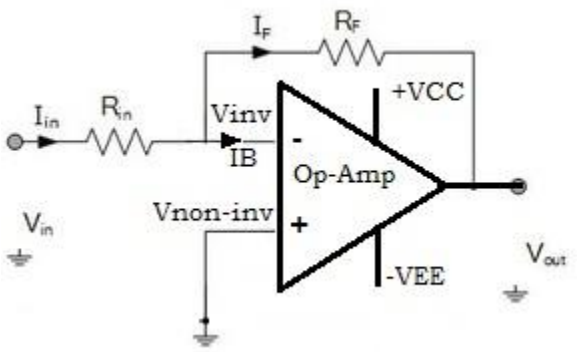


Figure 3: Op-amp Inverting amplifier circuit

The input signal is applied to the inverting terminal through R1 and the non-inverting terminal is connected to the ground, RF is the feedback(Negative feedback) resistor connected from the output terminal to the input terminal.

Applying KCL at inverting node,

$$I_{in} = I_B + I_F \quad ----------(1)$$

W.K.T., $I_B = 0$, Therefore

$$I_{in} = I_F \quad -------(2)$$

$$\frac{V_{in} - V_{inv}}{R_{in}} = \frac{V_{inv} - V_{out}}{R_F} \quad -----(3)$$

$$V_{non-inv} = 0, \text{therefore } V_{inv} = 0, \text{since Virtual ground}$$

Therefore,

$$\frac{V_{in}}{R_{in}} = -\frac{V_{out}}{R_F} \quad --------(4)$$

or

$$V_{out} = -V_{in}\left(\frac{R_F}{R_{in}}\right) \quad ------(5)$$

From equation (5), it has been observed that the output signal is R_F/R_{in} times that of the input signal with a negative sign indicates phase reversal.

$$\text{i.e., Gain } (A_v) = \frac{R_F}{R_{in}} \text{ ----- (6)}$$

Non-Inverting amplifier

An electronic circuit or device, which increases the strength of the input signal and the output signal is in phase with the input signal is called a non-inverting amplifier. Figure(4) shows the circuit diagram of the op-amp non-inverting amplifier.

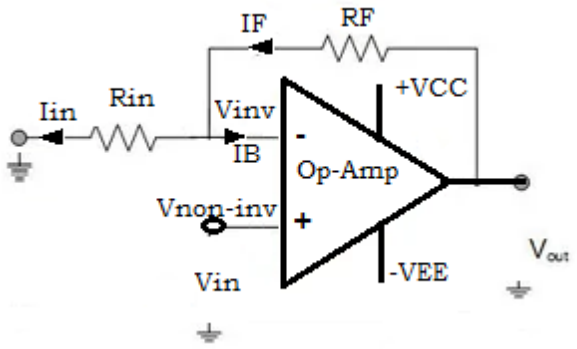


Figure 4: Op-amp Non-Inverting amplifier circuit

The input signal is applied to the non-inverting terminal and the non-inverting terminal is connected to the ground through R1, RF is the feedback(Negative feedback) resistor connected from the output terminal to the input terminal.

Applying KCL at inverting node,

$$I_F = I_B + I_{in} \text{ ---------- (7)}$$

W.K.T., $I_B = 0$, Therefore

$$I_{in} = I_F \text{ ------- (8)}$$

$$\frac{V_{inv} - 0}{R_{in}} = \frac{V_{out} - V_{inv}}{R_F} \text{ ----- (9)}$$

$V_{non-inv} = V_{in}$, therefore $V_{inv} = V_{in}$, since Virtual ground

Therefore,

$$\frac{V_{in}}{R_{in}} = \frac{V_{out} - V_{in}}{R_F} \text{ -------(10)}$$

$$V_{out} = +V_{in}\left(1 + \frac{R_F}{R_{in}}\right) \text{ -----(11)}$$

From equation (11), it has been observed that the output signal is $1+R_F/R_{in}$ times that of the input signal with a positive sign indicates the output is in-phase with the input signal.

$$\text{i.e., Gain } (A_v) = 1 + \frac{R_F}{R_{in}} \text{ ----- (12)}$$

Op-Amp summing amplifier

An electronic circuit or device, which amplifies the summation of two or more signals is called a summing amplifier. Figure(5) shows the circuit diagram of the op-amp summing amplifier for three inputs.

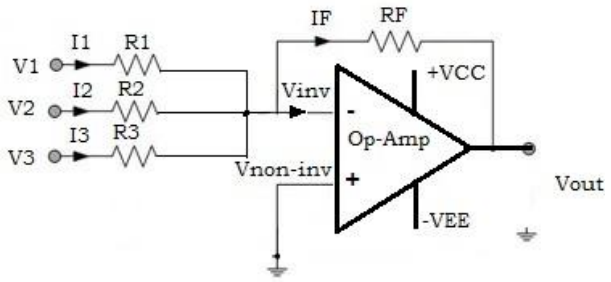


Figure 5: Op-amp summing amplifier circuit.

Input signals are applied to the inverting terminal through R1, R2, and R3, and the non-inverting terminal is connected to the ground, RF is the feedback(Negative feedback) resistor connected from the output terminal to the input terminal.

Applying KCL at inverting node,

$$I_1 + I_2 + I_3 = I_B + I_F ----------- (13)$$

W.K.T., $I_B = 0$, Therefore

$$I_1 + I_2 + I_3 = I_F ------- (14)$$

$$\frac{V_1 - V_{inv}}{R_1} + \frac{V_2 - V_{inv}}{R_2} + \frac{V_3 - V_{inv}}{R_3} = \frac{V_{inv} - V_{out}}{R_F} ----- (15)$$

$$V_{non-inv} = 0, \text{therefore } V_{inv} = 0, \text{since Virtual ground}$$

Therefore,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_{out}}{R_F} --------(16)$$

or

$$V_{out} = -(V_1 (\frac{R_F}{R_1}) + V_2 (\frac{R_F}{R_2}) + V_3 (\frac{R_F}{R_3})) ------(17)$$

if R_F=R_1=R_2=R_3,

$$V_{out} = -(V_1 + V_2 + V_3) ------(18)$$

From equation (18), it has been observed that the output signal is the negative sum of the input signals.

Op-Amp Difference amplifier

An electronic circuit or device, which amplifies the difference of two signals is called a difference amplifier and also called op-amp subtractor. Figure(6) shows the circuit diagram of the op-amp subtractor amplifier.

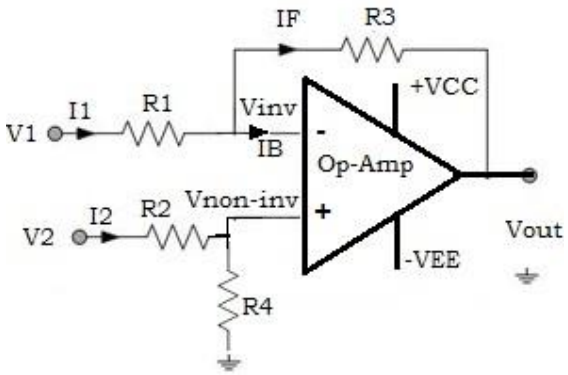


Figure 6: Op-amp Difference amplifier circuit.

Input signals are applied to the inverting terminal through R1, and the non-inverting terminal through R2, RF is the feedback(Negative feedback) resistor connected from the output terminal to the input terminal.

At inverting node,

$$I_1 = I_F \quad ---------(19)$$

$$\frac{V_1 - V_{inv}}{R_1} = \frac{(V_{inv} - V_{out})}{R_3} \quad ---------(20)$$

At the non-inverting node,

$$V_{non-inv} = I_2 R_4 \quad ---------(21)$$

$$V_{non-inv} = V_2 \left(\frac{R_4}{R_2 + R_4}\right) \quad ----(22)$$

$$V_{non-inv} = V_{inv}, \text{ since Virtual ground}$$

Determining V_{out} using superposition principle.

if V2=0;

$$V_{out} = -V_1 \left(\frac{R_3}{R_1}\right) \quad ---------(23)$$

if V1=0;

$$V_{out} = V_2 \left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right) \quad -----(24) \text{ (Since, Non-inverting amplifier)}$$

$$\text{therefore, } V_{out} == -V_1 \left(\frac{R_3}{R1}\right) + V_2 \left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right) \quad -----(25)$$

if $R_1 = R_2 = R_3 = R_4$

$$V_{out} = -V_1 + V_2 \quad -----(26)$$

From equation (18), it has been observed that the output signal is the difference between the two input signals.

Op-Amp Voltage follower

In an electronic circuit or device, the output signal is same as the input signal or output follows the input, such circuit is called voltage follower. The voltage follower circuit acts as a buffer.
Figure(7) shows the circuit diagram of the op-amp voltage follower.

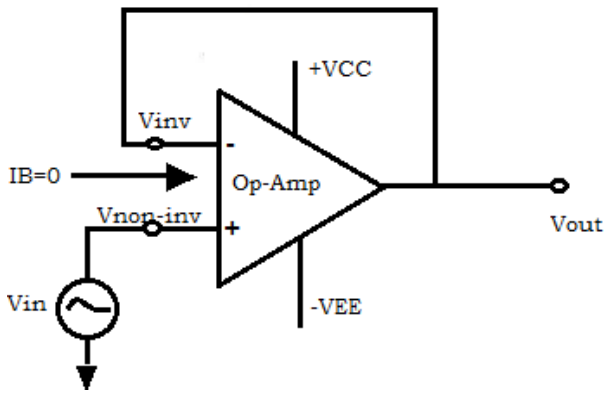


Figure 7: Op-amp voltage follower circuit.

Input signals are applied to the non-inverting terminal short-circuited the output terminal with the inverting terminal(feedback).

From the circuit,

$$V_{non-inv} = V_{in} - - - - - (27)$$
$$V_{inv} = V_{non-inv} = V_{in} - - - - - - - - - (28)$$

and

$$V_{out} = V_{inv} - - - - - - - - - - (29)$$

Therefore,

$$V_{out} = V_{in} - - - - - - (30)$$

Equation (30) shows that the output signal is equal to the input signal.

Op-Amp Integrator

An electronic circuit or device, which performs the integration of the input signal, is called an Integrator. Figure(8) shows the circuit diagram of the op-amp Integrator.

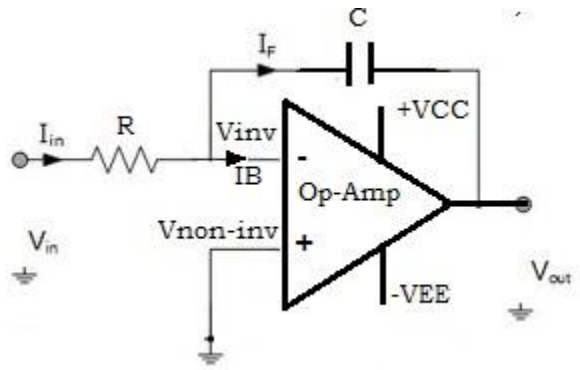


Figure 8: Op-amp Integrator circuit.

The input signal is applied to the inverting terminal through a resistor R and Capacitor C(Feedback element) is connected from the output terminal to inverting input terminal.

From the circuit,

$$I_{in} = I_F - - - - - (31)$$
$$\frac{(V_{in} - V_{inv})}{R} = C\frac{d}{dt}(V_{inv} - V_{out}) - - - - - - - (32)$$

We know that

$$V_{non-inv} = V_{inv} = 0 - - - - - (33)$$

(Since, Virtual Ground)

Therefore,

$$\frac{V_{in}}{R} = C\frac{d}{dt}(-V_{out}) - - - - - - - (34)$$

Integrating on both sides, we get

$$\int \frac{V_{in}}{R} dt = C\int \frac{d}{dt}(-V_{out})dt - - - - - - - (35)$$

$$V_{out} = -\frac{1}{RC}\int V_{in} dt - - - - - - - (36)$$

Equation (36) shows that the output signal is equal to the integral of the input signal.

1.6.6. Op-Amp Differentiator

An electronic circuit or device, which performs the Differentiation of the input signal, is called a Differentiator. Figure(9) shows the circuit diagram of the op-amp differentiator.

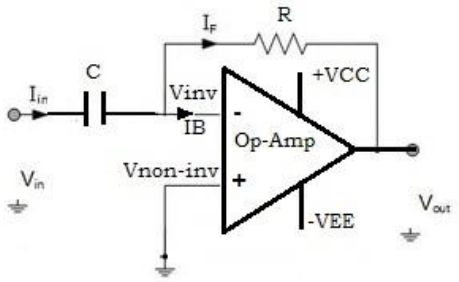


Figure 9: Op-amp differentiator circuit.

The input signal is applied to the inverting terminal through a resistor C and Resistor R (Feedback element) is connected from the output terminal to inverting input terminal.

From the circuit,

$$I_{in} = I_F \text{ ------ (37)}$$

$$C\frac{d}{dt}(V_{in} - V_{inv}) = \frac{(V_{inv} - V_{out})}{R} \text{ ------- (32)}$$

We know that

$$V_{non-inv} = V_{inv} = 0 \text{ ----- (38)} \quad \text{(Since, Virtual Ground)}$$

$$\text{Therefore, } C\frac{d}{dt}V_{in} = -\frac{V_{out}}{R} \text{ ------- (39)}$$

$$\text{or} \quad V_{out} = -RC\frac{d}{dt}V_{in} \text{ --------(40)}$$

Equation (40) shows that the output signal is equal to the derivative of the input signal.

EXCERCISE

1. **Draw the output waveforms for all types of signals as input.**

Wein Bridge Oscillator using Op-Amp

An electronic circuit that generates oscillations without oscillating input signal, such circuits are called oscillators. Wein bridge oscillator is a low frequency and type of RC oscillator, the resistors are connected in the form of Wein bridge, Hence the name Wein bridge oscillator. Figure (10) shows the circuit diagram of the Wein bridge oscillator.

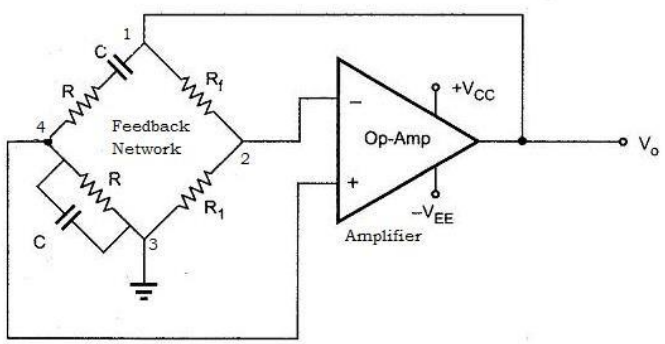


Figure 10: Wein Bridge oscillator

The output signal of the amplifier is fed back to the input through terminals 1 and 3 of the feedback network. Input to the amplifier stage is supplied from terminals 2 and 4 of the feedback network. Hence the amplifier output becomes the input voltage of the bridge whilst the output of the bridge becomes the input voltage of the amplifier. When the bridge is balanced the input voltage to the amplifier becomes zero, to produce the sustained oscillations input to the amplifier must be non-vanishing. Therefore the bridge is unbalanced by adjusting the proper values of the resistors. The RC network is responsible for determining the frequency of the oscillator.

$$\boldsymbol{f = \frac{1}{2\pi RC}}$$

Digital Electronics Fundamentals and Logic Gates.

Introduction

An electronic circuit, which processes the data or signals in the form of 0's and 1's is called Digital electronics. Digital signals or digital data are the groups of 0's and 1's, called binary number systems. Four major number systems are used to study and processing the digital systems or digital circuits, they are, Binary, Octal, Decimal, and Hexadecimal number systems. In the following section, the number systems and their conversions are explained.

Number systems

Binary Number system:

As the name implies, Bi means two, i.e., there are two symbols are used while representing the data in binary number systems. The symbols are 0 and 1. The binary number systems are also called as radix-2 system or weight -2 system.

Example: 0.1.,00,010,110101 ....

Octal Number system:

A Number system with eight symbols are called Octal number systems, the symbols of this system are 0,1,2,3,4,5,6,7.The octal number systems are also called radix-8 system or weight-8 system.

Example: 012, 345, 567, 345....

Decimal Number System:

A Number system with Ten symbols are called Decimal number systems, the symbols of this system are 0,1,2,3,4,5,6,7,8,9.The Decimal number systems are also called radix-10 systems or weight-10 systems.

Example: 9837, 1234, 9, 3234....

Hexadecimal Number System:

A Number system with 16 symbols are called Hexadecimal number systems, the symbols of this system are 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.The Hexadecimal number systems are also called radix-16 system or weight-16 system.

Example: 234, 01, 203A, ABF, DE4...

Number System Conversion

Decimal to Binary conversion

Every number has integer part and fractional part, for integer part successive division by two method and for fractional part successive multiplication by two method will be used to convert decimal number system into binary number system.

Example: $(345.75)_{10}=(?)_2$

Integer part: 345.

		Remainder
2	345	
2	172	-1
2	86	-0
2	43	-0
2	21	-1
2	10	-1
2	5	-0
2	2	-1
	1	-0

Note down
Bottom to top

i.e.,

$(345)_{10}=(101011001)_2$

Fractional part: 0.75

	Carry
0.75*2=1.5	-1
0.5*2=1.0	-1
0.0*2=0.0	-0
0.0*2=0.0	-0

Not down
Top to bottom

i.e.,

$(0.75)_{10}=(1100)_2$

Therefore,

$(345.75)_{10}=(101011001.\ 1100..)_2$

Decimal to Octal conversion

Every number has integer part and fractional part, for integer part successive division by eight method and for fractional part successive multiplication by eight method will be used to convert decimal number system into octal number system.

Example: $(3454.75)_{10}=(?)_8$

Integer part: 3454.

		Remainder
8	3454	
8	431	-6
8	53	-7
	6	-5

Note down
Bottom to top

i.e.,

$(3454)_{10}=(6576)_8$

Fractional part: 0.75

	Carry
0.75*8=6.0	-6
0.0*8=0.0	-0
0.0*8=0.0	-0
0.0*8=0.0	-0

Not down
Top to bottom

i.e.,

$(0.75)_{10}=(60)_8$

Therefore,

$(3454.75)_{10}=(6576.60..)_8$

Decimal to Hexadecimal conversion

Every number has integer part and fractional part, for integer part successive division by 16 method and for fractional part successive multiplication by 16 method will be used to convert decimal number system into octal number system.

Example: $(9554.85)_{10}=(?)_{16}$

Integer part: 9554.

Remainder

16 | 9554
16 | 597 -2
16 | 37 -5
2 -5

Note down Bottom to top

i.e.,

$(9554)_{10}=(2552)_{16}$

Fractional part: 0.85

Carry

0.85*16=13.6 -D
0.6*16=9.6 -9
0.6*16=9.6 -9
0.6*16=9.6 -9

Not down Top to bottom

i.e.,

$(0.85)_{10}=(D99)_{16}$

Therefore,

$(9554.85)_{10}=(2552.\ D99..)_{16}$

Binary to Decimal conversion

Multiplying sum of weighted binary numbers method is used to convert binary to decimal number system. For integer part positive weights and for fractional part negative weights will be considered.

Example: $(101011001.\ 1100)_2=(?)_{10}$

Bit position	8	7	6	5	4	3	2	1	0		-1	-2	-3
Bits	1	0	1	0	1	1	0	0	1	.	1	1	0
Weights	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}
Sum	$=1*2^8+0*2^7+1*2^6+0*2^5+1*2^4+1*2^3+0*2^2+0*2^1+1*2^0+1*2^{-1}+1*2^{-2}+0*2^{-3}$ $=345.75$												
Therefore, **$(101011001.\ 1100)_2=(345.75)_{10}$**													

Octal to Decimal conversion

Multiplying sum of weighted Octal numbers method is used to convert Octal to decimal number system. For integer part positive weights and for fractional part negative weights will be considered.

Example: $(6576.60)_8=(?)_{10}$

Bit position	3	2	1	0		-1	-2	-3
Digits	6	5	7	6	.	6	0	0
Weights	8^3	8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}
Sum	$=6*8^3+5*8^2+7*8^1+6*8^0+6*8^{-1}+0*8^{-2}+0*8^{-3}$ $=6576.75$							
Therefore, **$(6576.60)_8=(3454.75)_{10}$**								

Hexadecimal to Decimal conversion

Multiplying sum of weighted Hexadecimal numbers method is used to convert Hexadecimal to decimal number system. For integer part positive weights and for fractional part negative weights will be considered.

Example: $(2552.\ D99)_{16}=(?)_{10}$

Bit position	3	2	1	0		-1	-2	-3
Digits	2	5	5	2	.	D	9	9
Weights	16^3	16^2	16^1	16^0		16^{-1}	16^{-2}	6^{-3}
Sum	$=2*16^3+5*16^2+5*16^1+2*16^0+13*16^{-1}+9*16^{-2}+9*16^{-3}$ $=9555.9$							
Therefore, $(2552.\ D99)_8=(9555.9)_{10}$								

Octal to Binary conversion

Replacing the binary equivalent of each octal numbers to convert octal to binary. The following table shows the binary equivalent of each octal symbol.

Octal	Binary
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Example: $(67526.57)_8=(?)_2$

$(110111101010110.101111)_2$

Hexadecimal to Binary conversion

Replacing the binary equivalent of each Hexadecimal numbers to convert Hexadecimal to binary. The following table shows the binary equivalent of each Hexadecimal symbol.

Hexadecimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

Example: $(67AB26.5F)_{16}=(?)_2$

$(011001111010101100100110.01011111)_2$

Binary to Octal conversion

Group the given binary number into three bits format, for integer part from right to left and for fractional part left to right. Then replace 3 bits binary to its equivalent octal.
NOTE: If the number of bits are not enough to group, padding of zero's can be done.

Example: $(110111101010110).101111)_2 = (?)_8$

$$([110][111][101][010][110]).[101][111])_2 = (67526.57)_8$$

1.3.10.Binary to Hexadecimal conversion

Group the given binary number into four bits format, for integer part from right to left and for fractional part left to right. Then replace 4 bits binary to its equivalent Hexadecimal.

If the number of bits are not enough to group, padding of zero's can be done.

Example: $(011001111010101100100110.01011111)_2 = (?)_{16}$

$$([0110][0111][1010][1011][0010][0110].[0101][1111])_2 = (67AB26.5F)_{16}$$

Logic gates

Logic gates are the basic building blocks of any digital systems, it is an electronic circuits, which produces one output by taking one or more inputs. The relation between output to input/s are based on certain logic, the logic operations are named as AND, OR, NOT etc..

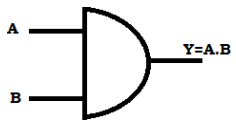
Logic gates are classified into two types.

i. Basic Gates

The logic gates which performs the basic operations, such as AND, OR and NOT are called basic gates.
a. AND gate
b. OR gate
c. NOT gate
these gates are explained as follows.

a. AND gate:

A logic gate, which performs logical AND operation is called AND gate. AND gates are having multiple input and single output. These gates produces logical value one, if all the inputs are one's else output is zero. Two inputs and single output gate is explained as follows.
Logic symbol:



Truth table:

Inputs		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Switching Equivalent Circuit:

The working principle of AND gate can be studies using it switching equivalent circuit, is as follows.

Circuit Diagram:

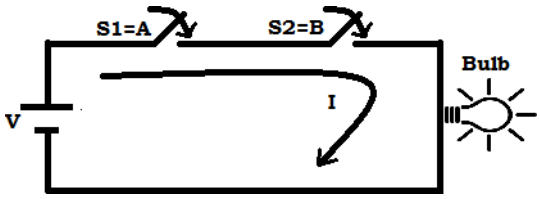


Figure: Switching Equivalent circuit

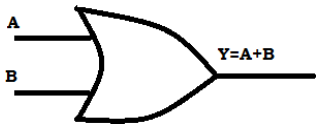
Explanation:

Figure shows the switching equivalent circuit of logical AND gate, which consisting of Voltage supply and series connected of two switches along with a bulb. Switches are considered as inputs A and B.
case(i): If A=0 and B=0, i.e., two switches are in open state, the complete circuit is open circuit. Hence current will not flow through the circuit and energy will not be supplied to bulb, so the bulb will not glow. Hence, output Y=0.
case(ii): If A=0 and B=1, i.e., Switch A is open and Switch B is closed, the complete circuit is open circuited. hence current will not flow through the circuit and energy will not be supplied to the bulb, so the bulb will not glow. Hence, output Y=0.
case(iii): If A=1 and B=0, i.e., Switch A is Closed and Switch B is Open, the complete circuit is open circuited. hence current will not flow through the circuit and energy will not be supplied to the bulb so the bulb will not glow. Hence, output Y=0.
case(iv): If A=1 and B=1, i.e., two switches are in closed state, current will flow through the circuit and energy will supply to the bulb, so the bulb will glow. Hence, output Y=1.

b. OR gate:

A logic gate, which performs logical OR operation is called OR gate. OR gates are having multiple input and single output. These gates produces logical value one, if any one of the input is logical one, if all the input are zero's then the output is zero. Two inputs and single output gate is explained as follows.

Logic symbol:



Truth table:

Inputs		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Switching Equivalent Circuit:

The working principle of AND gate can be studies using it switching equivalent circuit, is as follows.

Circuit Diagram:

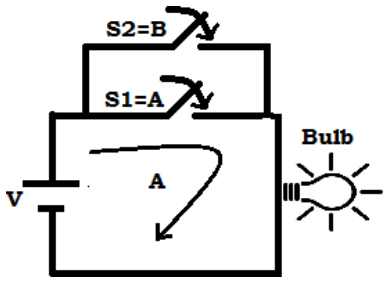


Figure: Switching Equivalent circuit

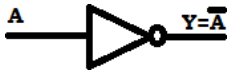
Explanation:

Figure shows the switching equivalent circuit of logical NOT gate, which consisting of Voltage supply and series connected of two switches along with a bulb. Switches are considered as inputs A and B.
case(i): If A=0 and B=0, i.e., two switches are in open state, the complete circuit is open circuit. Hence current will not flow through the circuit and energy will not be supplied to bulb, so the bulb will not glow. Hence, output Y=0.
case(ii): If A=0 and B=1, i.e., Switch A is open and Switch B is closed, the circuit is closed. hence current will flow through the circuit and energy will be supplied to the bulb, so the bulb will glow. Hence, output Y=1.
case(iii): If A=1 and B=0, i.e., Switch A is Closed and Switch B is Open, the circuit is closed. hence current will flow through the circuit and energy will be supplied to the bulb so the bulb will glow. Hence, output Y=1.
case(iv): If A=1 and B=1, i.e., two switches are in closed state, current will flow through the circuit and energy will supply to the bulb, so the bulb will glow. Hence, output Y=1.

c. NOT gate:

A logic gate, which performs logical NOT operation is called NOT gate. NOT gates are single input and single output gates. These gates produces logical value one, if the input is zero and output is zero if the input is one. NOT gate is explained as follows.

Logic symbol:



Truth table:

Input	Output
A	$Y=\bar{A}$
0	1
1	0

Switching Equivalent Circuit:

The working principle of AND gate can be studies using it switching equivalent circuit, is as follows.

Circuit Diagram:

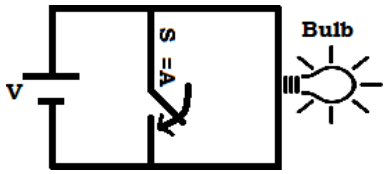


Figure: Switching Equivalent circuit

Explanation:

Figure shows the switching equivalent circuit of logical NOT gate, which consisting of Voltage supply and series connected of two switches along with a bulb. Switches are considered as inputs A and B.
case(i): If A=0, i.e., Switch A is open and the circuit is closed. hence current will flow through the circuit and energy will be supplied to the bulb, so the bulb will glow. Hence, output Y=1.
case(ii): If A=1 i.e., two switch A is closed, the energy will not supply to the bulb, so bulb will not glow and hence the output Y=0.

ii. Derived Gates:

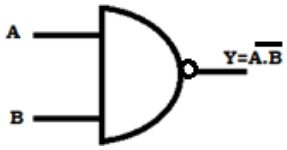
The gates are designed by using the basic gates are called derived gates. There are four types of derived gates, they are.
a. NAND gate
b. NOR gate
c. EXOR gate
d. EXNOR gate.

The logic symbols and truth tables of all these gates are as follows.

a. NAND gate:

A logic gate, which performs logical NOT of AND operation is called NAND gate. NAND gates are having multiple input and single output. These gates produces logical value zero, if all the inputs are one's otherwise output is one. Two inputs and single output gate is explained as follows.

Logic Symbol:



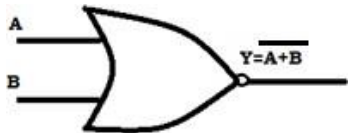
Truth Table:

Inputs		Output
A	B	$Y=\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

a. NOR gate:

A logic gate, which performs logical NOT of OR operation is called NOR gate. NOR gates are having multiple input and single output. These gates produces logical value one, if all the inputs are zero's otherwise output is zero. Two inputs and single output gate is explained as follows.

Logic Symbol:



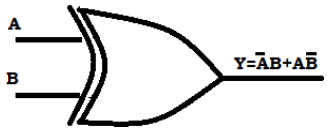
Truth Table:

Inputs		Output
A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

c. EXOR Gate:

A logic gate, which performs logical Exclusive OR operation is called EXOR gate. EXOR gates are having multiple input and single output. These gates produces logical value zero, if all the inputs are 0's or 1's otherwise output is one. Two inputs and single output gate is explained as follows.

Logic Symbol:



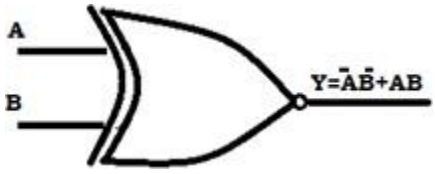
Truth Table:

Inputs		Output
A	B	$Y=\overline{A+B}$
0	0	0
0	1	1
1	0	1
1	1	0

d. EXNOR gate:

A logic gate, which performs logical Exclusive NOT of OR operation is called EXNOR gate. EXNOR gates are having multiple input and single output. These gates produces logical value one, if all the inputs are 0's or 1's otherwise output is zero. Two inputs and single output gate is explained as follows.

Logic Symbol:

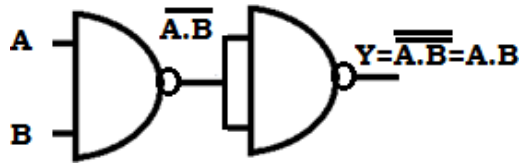


Truth Table:

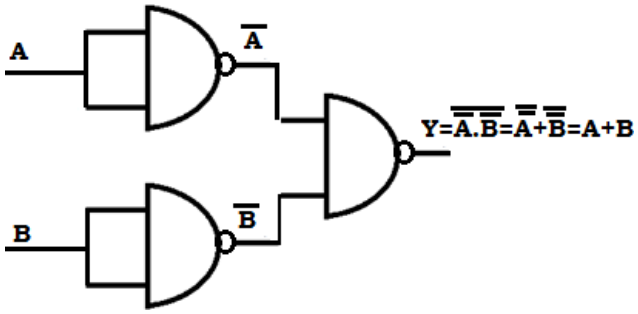
Inputs		Output
A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	1

NOTE: NAND and NOR gates are called UNIVERSAL gates, because all the basic gates can be realized by using either NAND or NOR gates only.

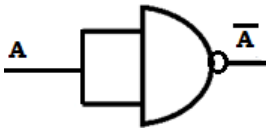
i) Realization of AND gate using NAND gates only.



ii) Realization of OR gate using NAND gates only.



iii) Realization of NOT gate using NAND gate.



Boolean Algebra

Performing algebraic operations using truth values is called Boolean algebra. The truth values are either true or false in other words binary logic levels either 0 or 1.

Boolean algebra helps to simplify the logical expressions and hence helps for designing the logical circuits.

Rules of Boolean algebra:

1. Commutative Law
(a) A + B = B + A
(b) A B = B A

2. Associate Law
(a) (A + B) + C = A + (B + C)
(b) (A B) C = A (B C)

3. Distributive Law
(a) A (B + C) = A B + A C
(b) A + (B C) = (A + B) (A + C)

4. Identity Law
(a) A + A = A
(b) A A = A

5.

(a) $AB + A\bar{B} = A$
(b) $(A + B)(A + \bar{B}) = A$

6. Redundance Law
(a) $A + A B = A$
(b) $A (A + B) = A$

7.
(a) $0 + A = A$
(b) $0 A = 0$
8.
(a) $1 + A = 1$
(b) $1 A = A$

9.
(a) $\bar{A} + A = 1$
(b) $\bar{A} A = 0$

10.
(a) $A + \bar{A} B = A + B$
(b) $A(\bar{A} + B) = AB$

11. De Morgan's Theorem
(a) $\overline{AB} = \bar{A}\bar{B}$
(b) $\overline{AB} = \bar{A} + \bar{B}$

Proof of De Morgan's laws.

Theorem-1: Complement of the sum of the two or more variables is equal to the product of the complements of their variables.

Proof:

A	B	$\bar{A}$	$\bar{B}$	LHS=$\overline{A+B}$	RHS=$\bar{A}\bar{B}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

Theorem-2: Complement of the product of the two or more variables is equal to the sum of the complements of their variables.

Proof:

A	B	$\bar{A}$	$\bar{B}$	LHS=$\overline{AB}$	RHS=$\bar{A}+\bar{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

Important mathematical expressions on semiconductor diode:

1. Diode Current Equation:

$$I_F = I_o\,(e^{\frac{v}{\eta V_T}} - 1) \quad ---------(1)$$

Where, I_F is the diode forward current, I_o is the reverse saturation current, η is a constant, 1for Germanium and 2 for Silicon diodes, V is the voltage drop across the diode during conduction mode(Forward Biasing) and V_T is the volt equivalent Temperature given by,

$$V_T = \frac{kT}{q} \quad ---------- (2)$$

Where, k is the Boltzmann's constant (1.380649×10^{-23}J/K), T is the temperature in Kelvin and q is the charge of an electron ($1.602x10^{-19}$ C).

V and I_o are temperature dependent variables.

(i). I_o doubles for every 10°C rise in temperature.

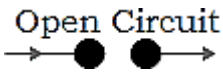
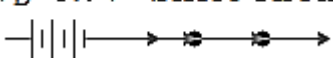
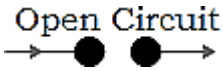
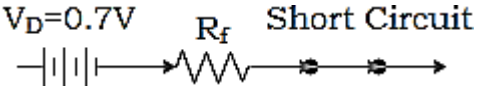
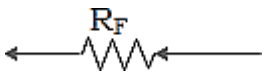
$$\text{i.e., } I_{02} = I_{01}x\,2^{\frac{t2-t1}{10}} \quad ---------- (3)$$

Where, I_{o2} is the reverse saturation current at temperature t_2°C and I_{o1} is the reverse saturation current at t_1°C.

(ii). V reduces by 2.5mV for every 1°C rise in temperature.

$$\text{i.e., } v_{F2} = v_{F_1} - 2.5x10^{-3}x(t_2 - t_1) \quad ----------(4)$$

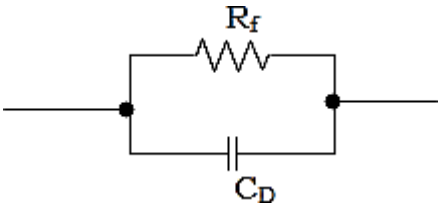
2. Diode's DC equivalent circuits

Forward Bias	Reverse Bias
Ideal model Short Circuit 	**Ideal model** Open Circuit 
Simplified model V_D=0.7V Short Circuit 	**Simplified model** Open Circuit 
Approximate model (piece-wise linear approximation) V_D=0.7V R_f Short Circuit 	**Approximate model (piece-wise linear approximation)** R_F 

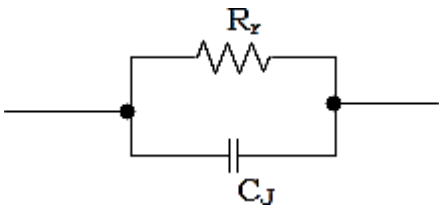
NOTE: V_F=0.3V for Germanium diodes.

3. Diode's AC equivalent circuits

Forward Bias	Reverse Bias



$$C_D = \frac{dQ}{dV}$$



$$C_J = \frac{sA}{W}$$

NOTE: Dielectric Constant for Si diode is 11.9 and and for Geermanium diode is 16.0