GANDHI INSTITUTE OF TECHNOLOGY AND MANAGEMENT

Lesson Plan

Name of the Program	**Diploma in ElectricalEngineering**				
Course Name	**DIGITAL ELECTRONICS & MICROPROCESSOR**			Course Code	**C303**
Course Year	**Third**	Semester	**5rd**	Academic Period	**2022-23**
No. of Classes allotted per Week	**05**	Planned Classes Required to Complete the Course			**60**

Sl. No.	Topics to be covered	Module	No. of hoursRequired	Mode of Teaching
1	Basics Of Digital Electronics	I	01	LM/ IM
2	Binary, Octal, Hexadecimal number systems and compare with Decimal system.	I	03	LM/ IM
3	Binary addition, subtraction, Multiplication and Division.	I	01	LM/ IM
4	1‘s complement and 2‘s complement numbers for a binary number	I	02	LM/ IM/ ICT
5	Subtraction of binary numbers in 2‘s complement method.	I	02	LM/ IM
6	Use of weighted and Un-weighted codes	I	01	LM/ IM
7	Write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.	I	01	LM/ IM
8	Importance of parity Bit.	I	02	LM/ IM/ ICT
9	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.	I	02	LM/ IM
10	Realize AND, OR, NOT operations using NAND, NOR gates.	I	02	LM/ IM
11	Different postulates and De-Morgan‘s theorems in Boolean algebra.	I	01	LM/ IM
12	Simple problems on above	I	01	LM/ IM
13	Use Of Boolean Algebra For Simplification Of Logic Expression	I	03	LM/ IM
14	Karnaugh Map For 2,3,4 Variable, Simplification Of SOP Logic Expression Using K-Map.	I	03	LM/ IM
15	Karnaugh Map For 2,3,4 Variable, Simplification Of POS Logic Expression Using K-Map.	I	02	LM/ IM
16	Give the concept of combinational logic circuits.	II	03	LM/ IM/ ICT
17	Half adder circuit and verify its functionality using truth table	II	01	LM/ IM
18	Realize a Half-adder using NAND gates only and NOR gates only.	II	03	LM/ IM/ ICT
19	Full adder circuit and explain its operation with truth table.	II	02	LM/ IM
20	Realize full-adder using two Half-adders and an OR – gate and write truth table	II	04	LM/ IM

21	Full subtractor circuit and explain its operation with truth table.	II	02	LM/ IM
22	Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer	II	01	LM/ IM/ ICT
23	Working of Binary-Decimal Encoder & 3 X 8 Decoder.	II	02	LM/ IM
24	Working of Two-bit magnitude comparator.	II	02	LM/ IM
25	Solve simple problems.	II	02	LM/ IM
26	Give the idea of Sequential logic circuits.	III	01	LM/ IM/ ICT
27	State the necessity of clock and give the concept of level clocking and edge triggering,	III	01	LM/ IM
28	Clocked SR flip flop with preset and clear inputs.	III	01	LM/ IM
29	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table	III	02	LM/ IM
30	Concept of race around condition and study of master slave JK flip flop	III	01	LM/ IM/ ICT
31	Give the truth tables of edge triggered D and T flip flops and draw their symbols.	III	01	LM/ IM
32	Applications of flip flops. Define modulus of a counter	III	01	LM/ IM
33	4-bit asynchronous counter and its timing diagram	III	02	LM/ IM
34	Asynchronous decade counter. 4-bit synchronous counter.	III	02	LM/ IM/ ICT
35	Distinguish between synchronous and asynchronous counters.	III	01	LM/ IM
36	State the need for a Register and list the four types of registers.	III	01	LM/ IM
37	Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.	III	01	LM/ IM
38	Introduction to Microprocessors, Microcomputers	IV	01	LM/ IM
39	Architecture of Intel 8085A Microprocessor and description of each block	IV	01	LM/ IM
40	Pin diagram and description.Stack, Stack pointer & stack top	IV	01	LM/ IM
41	Interrupts, Opcode & Operand	IV	01	LM/ IM
42	Differentiate between one byte, two byte &three byte instruction with example.	IV	01	LM/ IM
43	Instruction set of 8085 example,	IV	01	LM/ IM
44	Addressing mode, Fetch Cycle, Machine Cycle, Instruction Cycle, T-State	IV	01	LM/ IM
45	Timing Diagram for memory read, memory write, I/O read, I/O write	IV	01	LM/ IM
46	Timing Diagram for 8085 instruction	IV	01	LM/ IM
47	Counter and time delay, Simple assembly language programming of 8085	IV	01	LM/ IM
48	Basic Interfacing Concepts, Memory mapping & I/O mapping	V	01	LM/ IM

49	Functional block diagram and description of each block of Programmable peripheral interface Intel 8255	V	01	LM/ IM
50	Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller	V	01	LM/ IM

Signature of the Faculty **Signature of the HoD**